

CGP-100 Graphics Processor

Logic Diagrams

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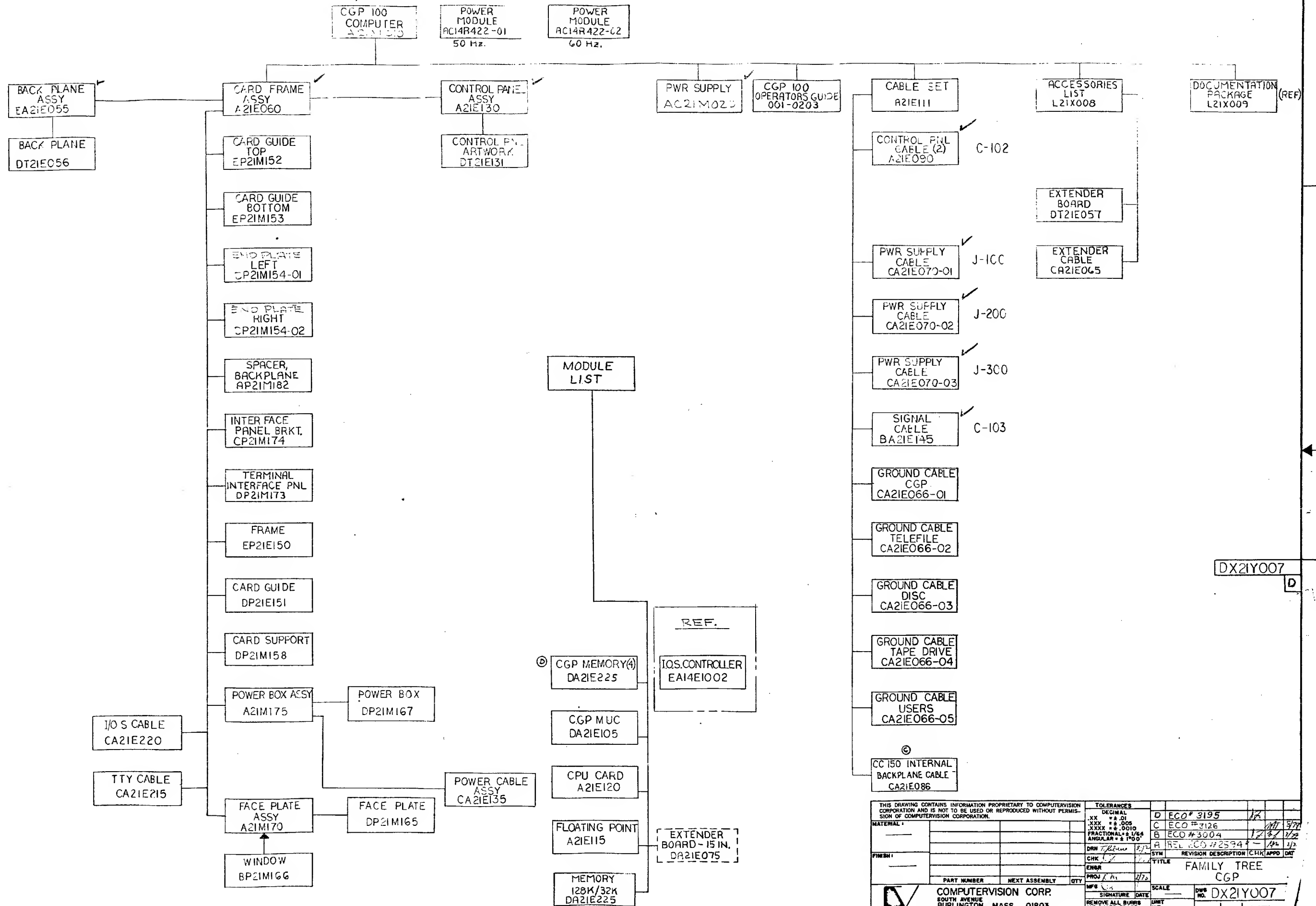
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CGP Family Tree



DX21Y007
D

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.				TOLERANCES							
				XX	DECIMAL	± .01		D	ECO # 3195	1/2	
				XXX	± .005			C	ECO # 3126	1/2	3/77
				XXXX	± .0010			B	ECO # 3004	1/2	3/77
				FRACTIONAL	± 1/64			A	REL ECO # 2594	1/2	3/77
				ANGULAR	± 1°00'						
				CHK	DATE			SYN	REVISION DESCRIPTION	CHK	APPD
				ENG				TITLE	FAMILY TREE CGP		
				PROJ	DATE			PART NUMBER			
				SCALE				NEXT ASSEMBLY			
				QTY				UNIT			
				REMOVE ALL BURRS AND SHARP EDGES				SHEET	1 OF 1 SHEETS		
				COMPUTERVISION CORP.				SCALE	DWS NO. DX21Y007		
				SOUTH AVENUE				DATE			
				BURLINGTON, MASS. 01803				UNIT			

Backplane

Connector List
Artwork Silkscreen

POWER SUPPLY CONNECTORS

16	14	12	10	8	6	4	2
-5V	-12V	-5V	-12V	-5V	-12V	-5V	-12V
15	13	11	9	7	5	3	1

J100 J200 J300

TTY CONNECTOR

J1, J2, J4, J5, J6

5	4	3	2	1
-5V	-12V	-5V	-12V	-5V
9	8	7	6	5

PUNCH

20	19	18	17	16	15	14	13	12	11
GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
1	2	3	4	5	6	7	8	9	10

H1 SPEED READER

20	19	18	17	16	15	14	13	12	11
GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
1	2	3	4	5	6	7	8	9	10

J9-J14

1	A61	14
2	A63	15
3	A65	16
4	A67	17
5	A71	18
6	A73	19
7	A75	20
8	A77	21
9	A81	22
10	A83	23
11	A85	24
12	A87	25
13	A91	26

TYPE	SLT	POS	CONN
TTY	1	J1	
TTY	2	J2	
TTY	3	J4	
TTY	4	J5	
TTY	5	J6	
TTY	6	J9	
TTY	7	J10	
TTY	8	J11	
TTY	9	J12	
TTY	10	J13	
TTY	11	J14	
TTY	12	J7	
TTY	13	J8	
TTY	14	J1	
TTY	15	J2	
TTY	16	J4	
TTY	17	J5	
TTY	18	J6	
TTY	19	J9	
TTY	20	J10	
TTY	21	J11	
TTY	22	J12	
TTY	23	J13	
TTY	24	J14	
TTY	25	J7	
TTY	26	J8	

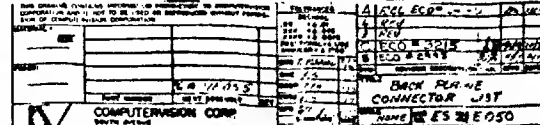
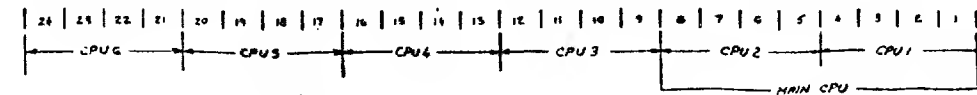
SLOTS 6,7,8,13,14,15,16,21,22,23,24

SLOT 5, (ONLY)

SLOTS 4,8,12,16,20,24

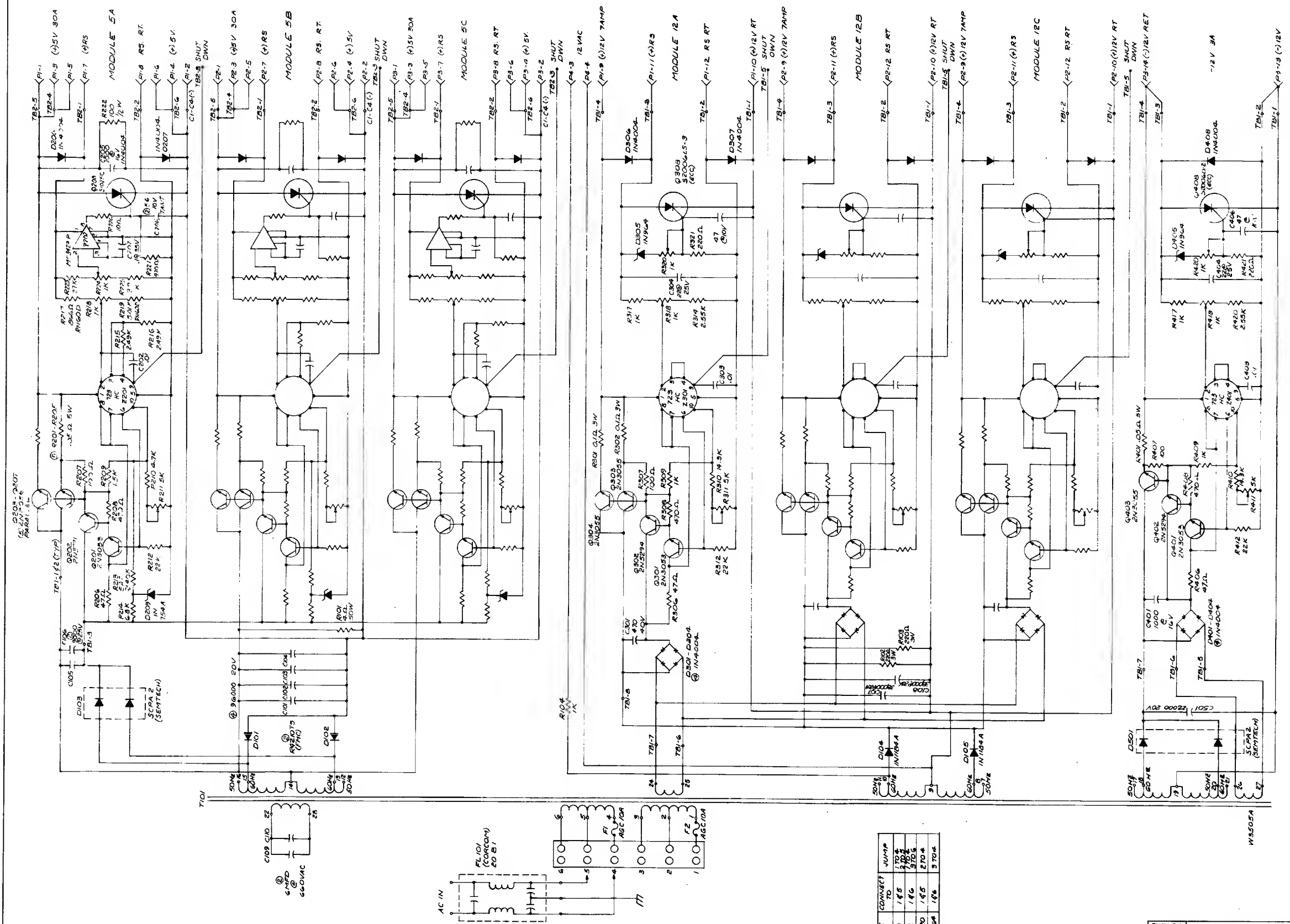
SLOTS 3,11,19

SLOTS 2,10,18



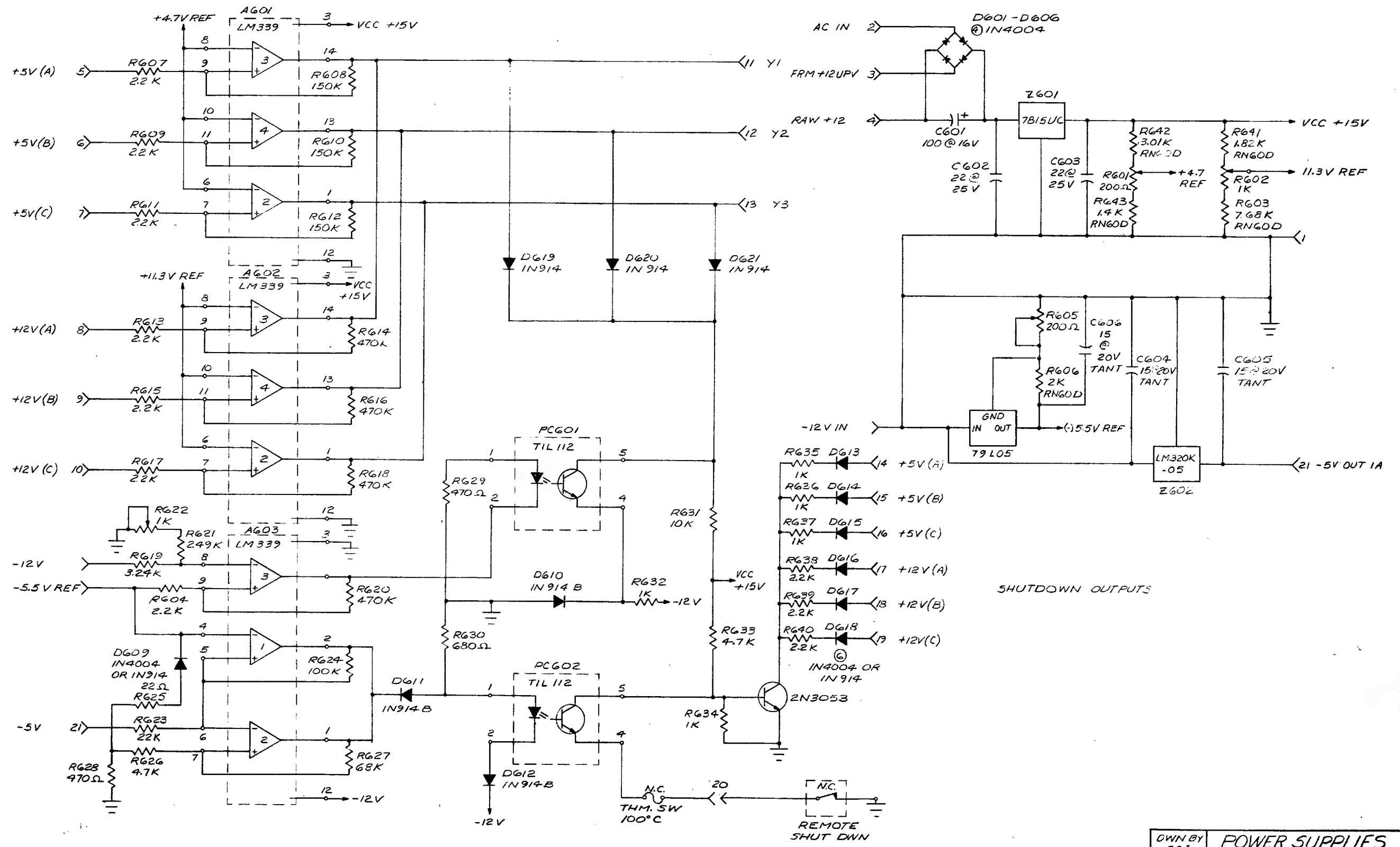
Power Supply

	<u>Sheet No.</u>
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Regulator Modules	1
Logic Module	2
– 5 Volt Regulator	2



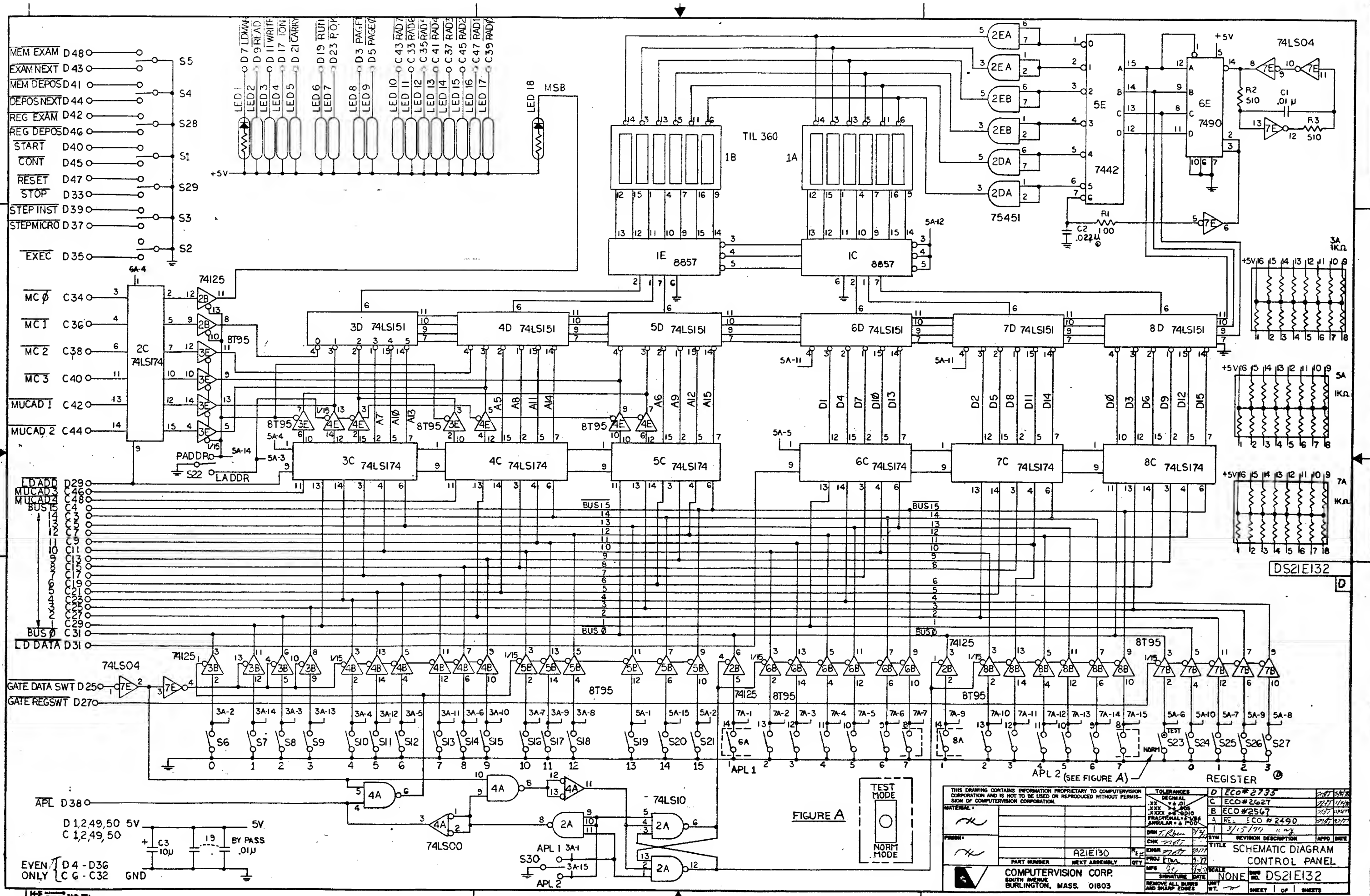
AC LINE	CONNECT	TO	VOLTS
80 TO 110	1.5	1.5	1.5
110 TO 120	1.5	1.5	1.5
120 TO 130	1.5	1.5	1.5
130 TO 140	1.5	1.5	1.5
140 TO 150	1.5	1.5	1.5
150 TO 160	1.5	1.5	1.5
160 TO 170	1.5	1.5	1.5
170 TO 180	1.5	1.5	1.5
180 TO 190	1.5	1.5	1.5
190 TO 200	1.5	1.5	1.5

POWER SUPPLIES
WALLINGFORD, CONN.
SCHEMATIC
PS11152B SH1



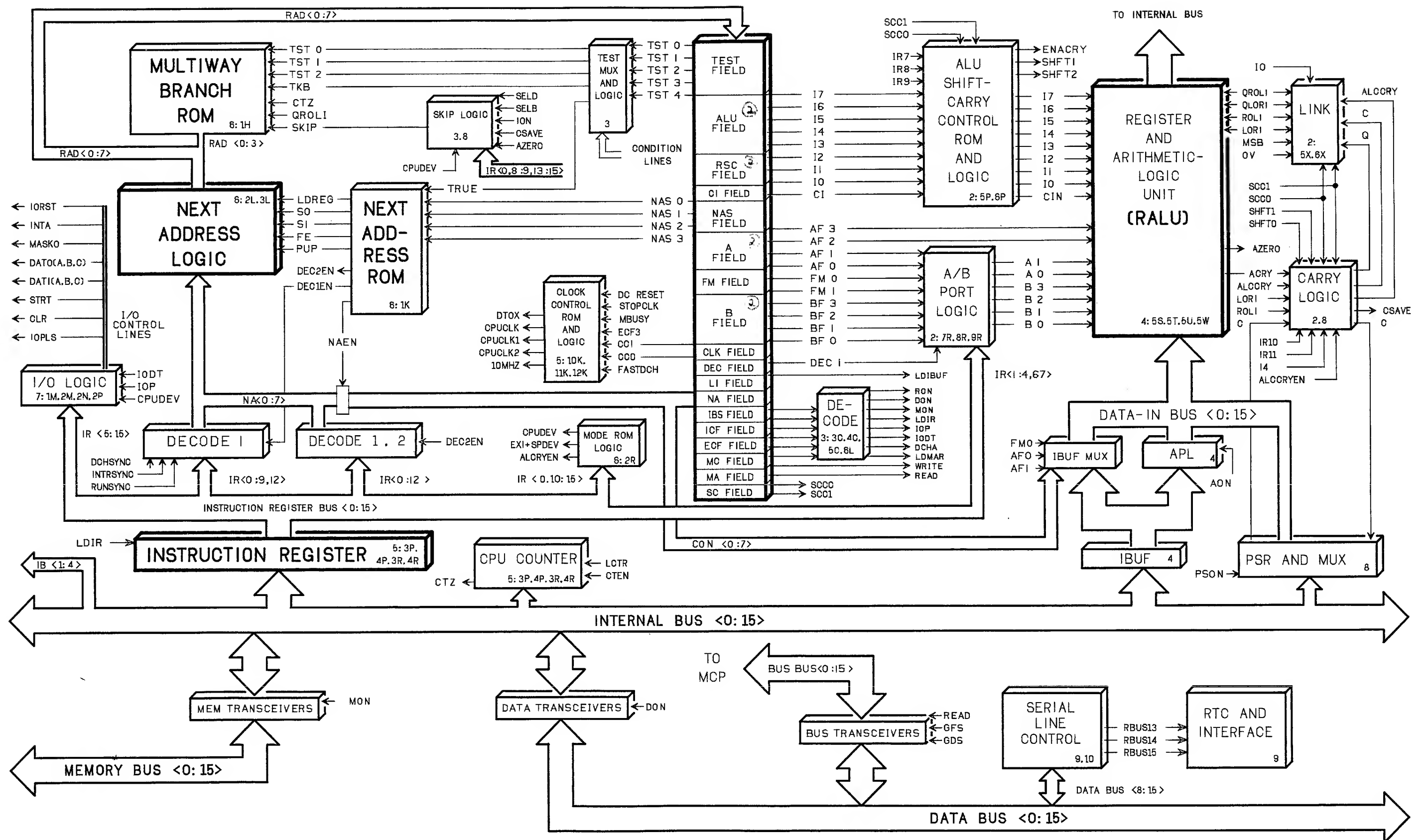
Control Panel

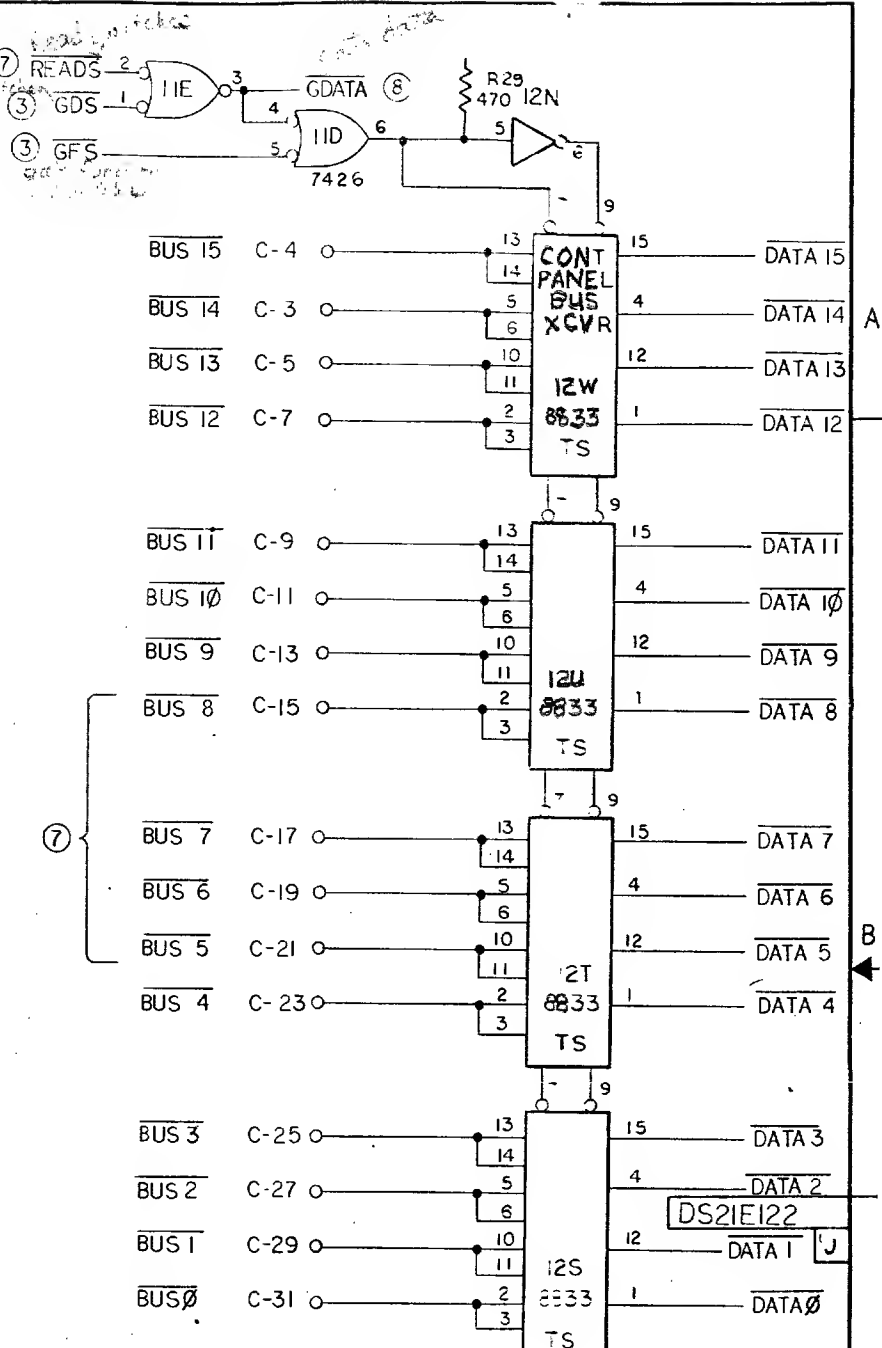
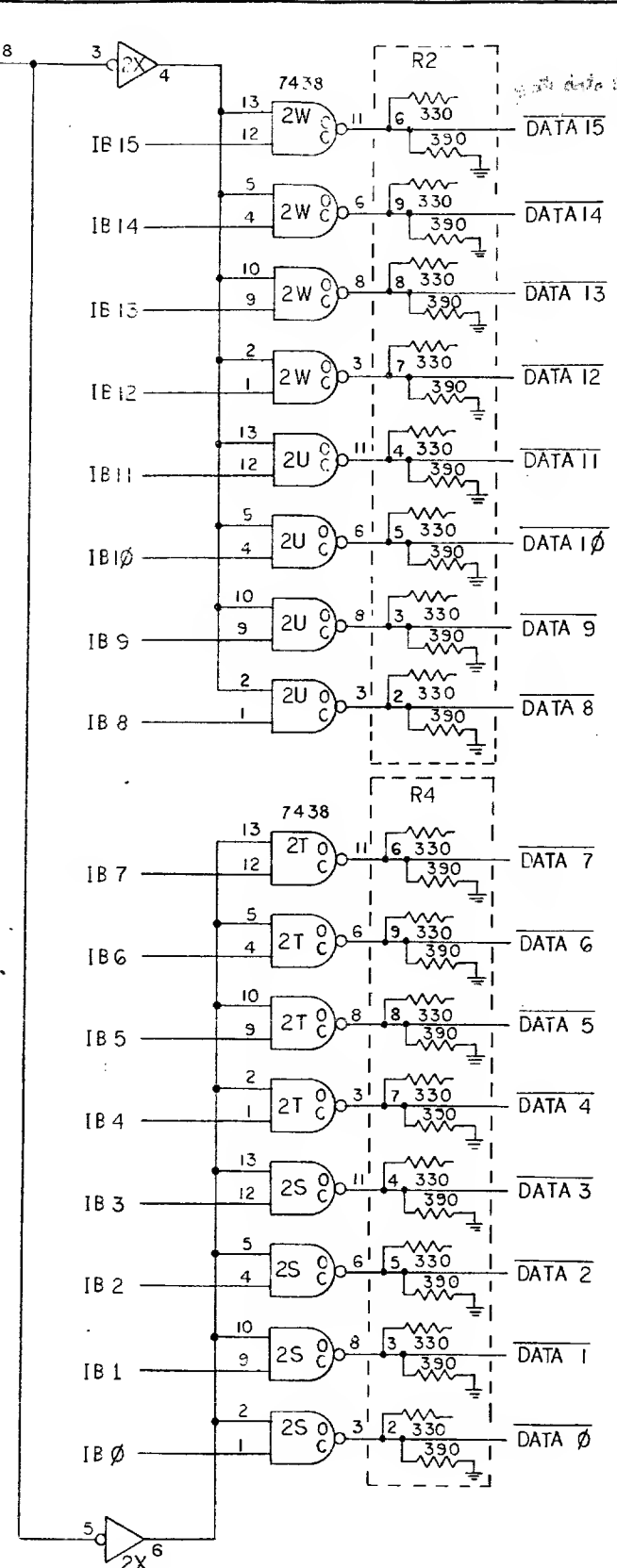
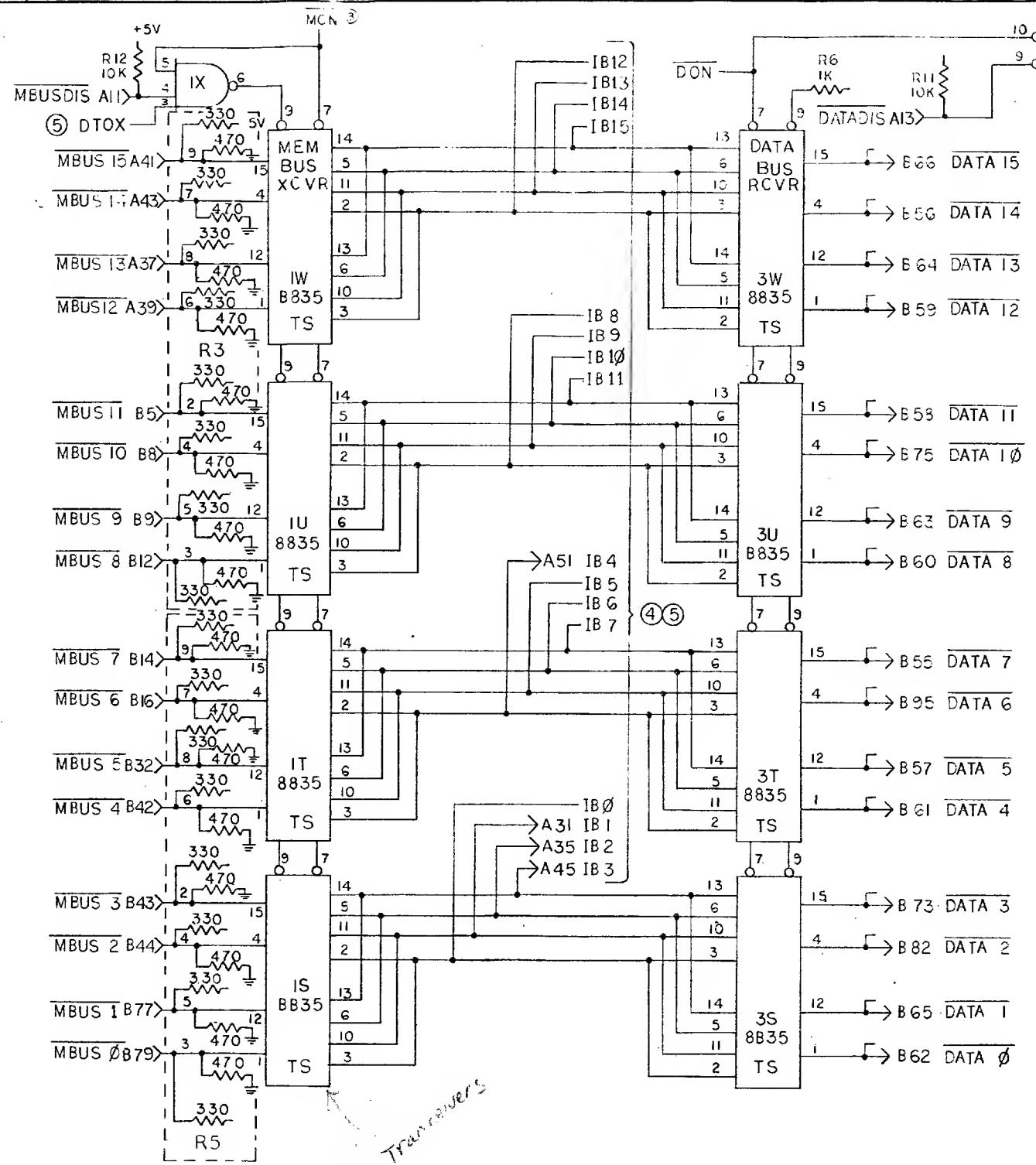
Logic Diagram



Central Processor Unit

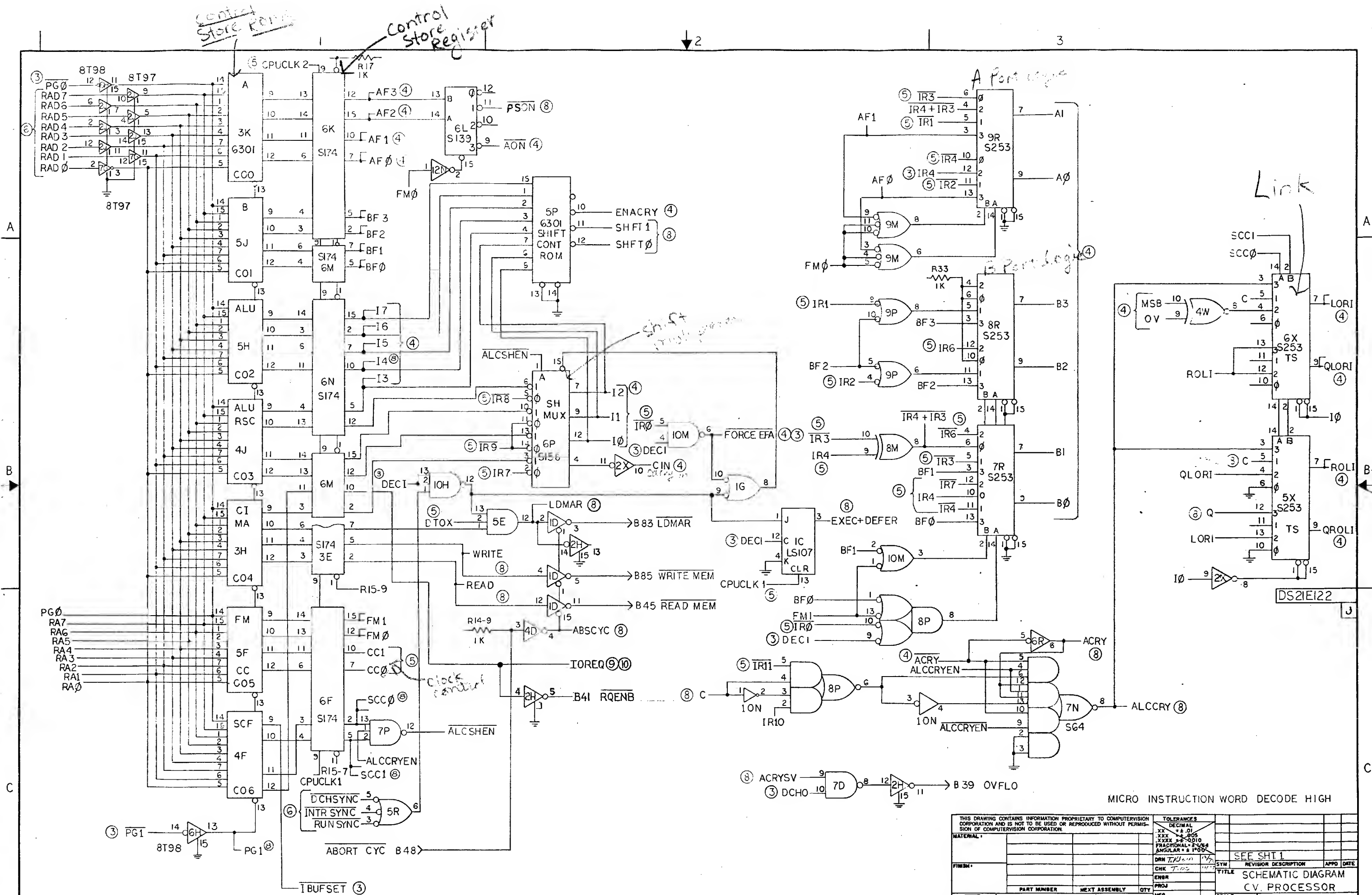
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Control Panel Interface	8
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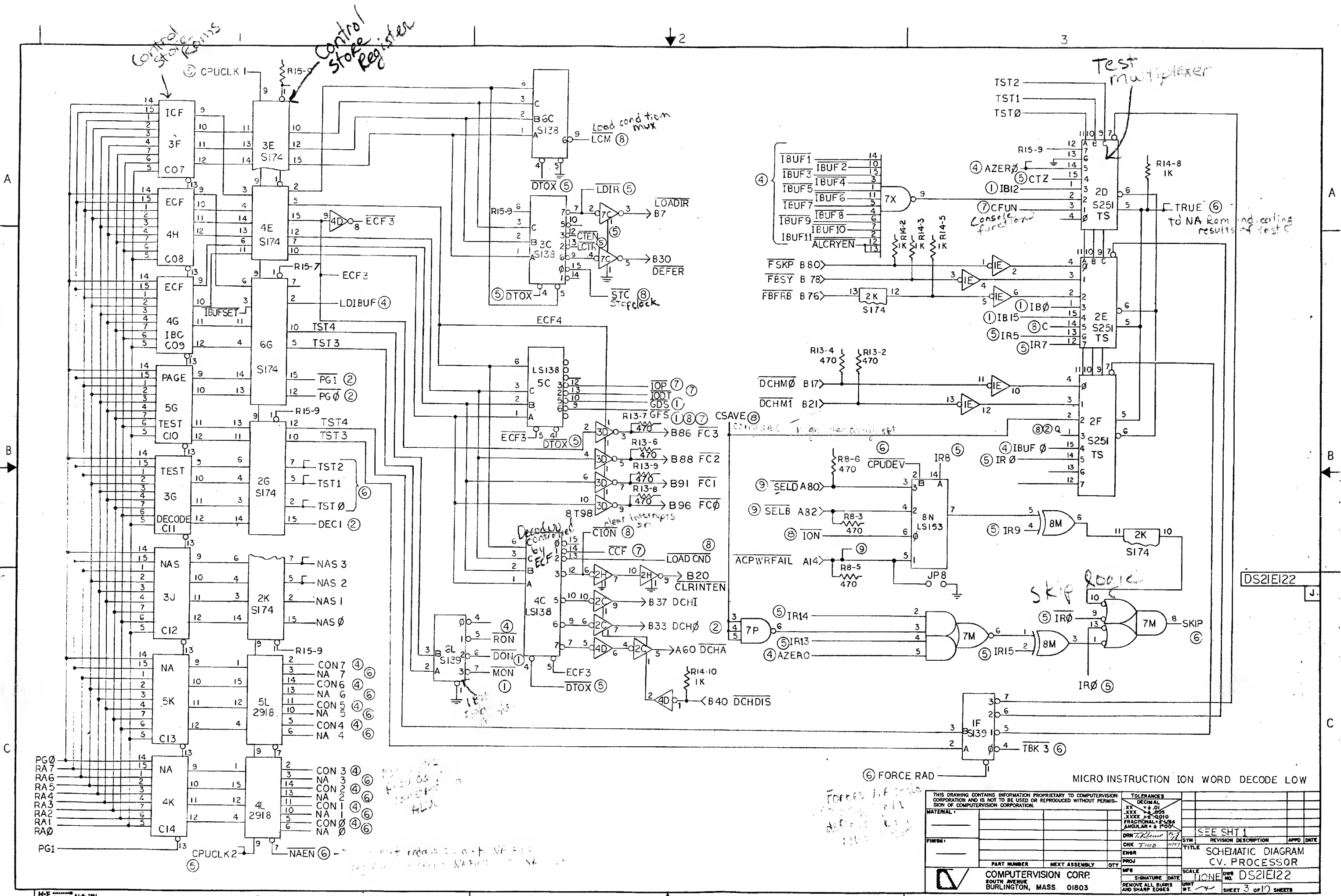




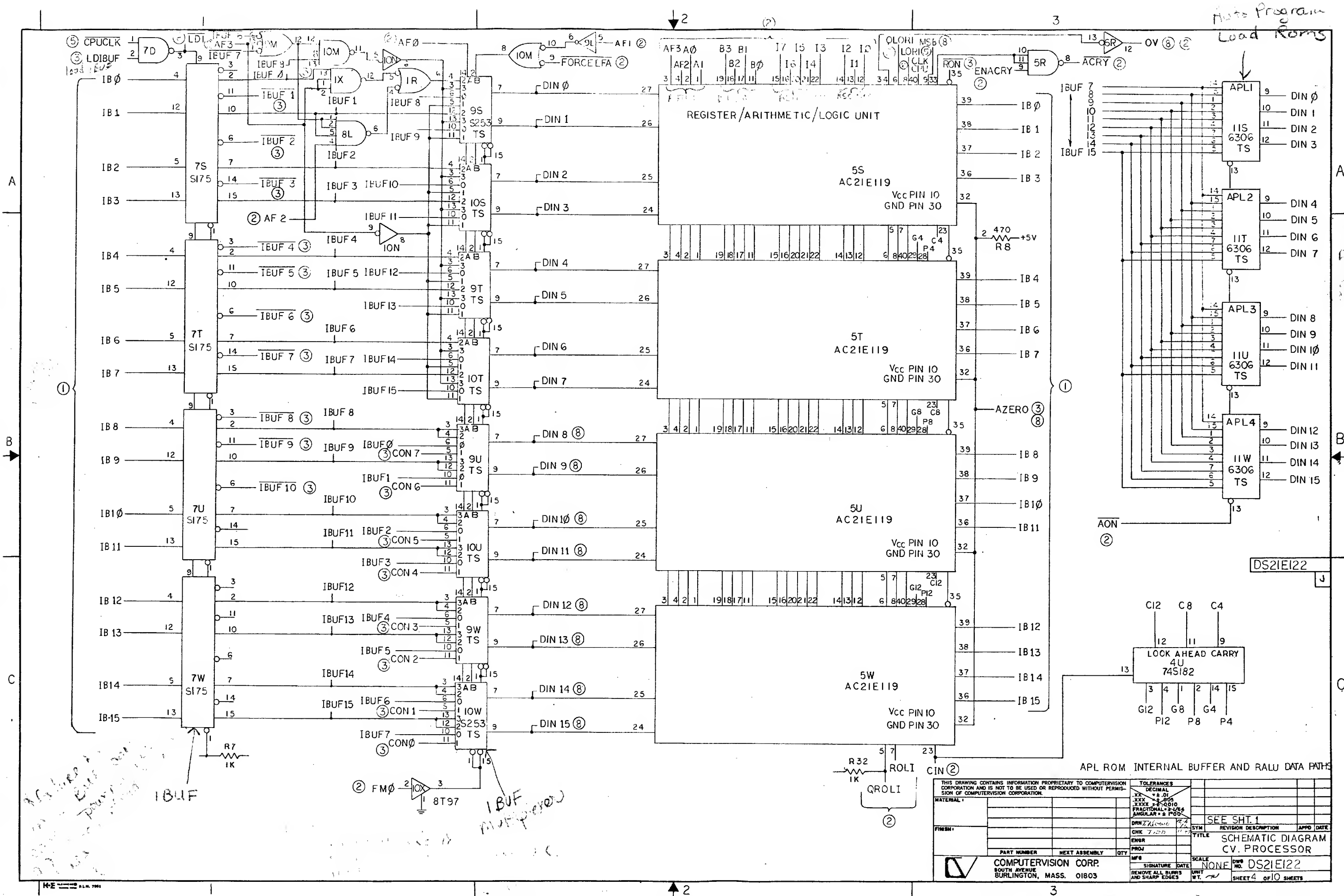
CONTROL PNL. BUS & DATA AND MEMORY BUS DRIVERS

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.		TOLERANCES	J	ECO # 3298	1/2 1/2 1/2
		DECIMAL	XX	ECO # 2745	1/2 1/2 1/2
		FRACTIONAL	XX	ECO # 2700	1/2 1/2 1/2
		ANGULAR & POS.	XX	REL ECO # 2597	1/2 1/2 1/2
		DRN	XX	RELEASE ECO 2577	1/2 1/2 1/2
		CHK	XX	REVISION DESCRIPTION	CHK APPD DATE
		ENGR	XX	TITLE	SCHEMATIC DIAGRAM
		PROJ	XX	C.V. PROCESSOR	
		PART NUMBER	DT2IE121	SCALE	NONE
		NEXT ASSEMBLY		DWG NO.	DS2IE122
		QTY		UNIT	SHEET 1 OF 10 SHEETS
		COMPUTERVISION CORP.			
		SOUTH AVENUE			
		BURLINGTON, MASS. 01803			



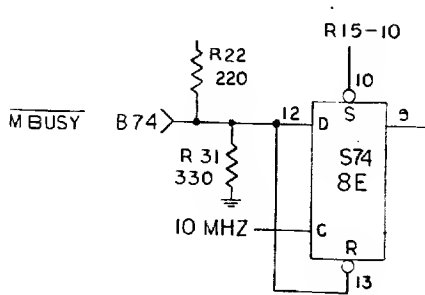
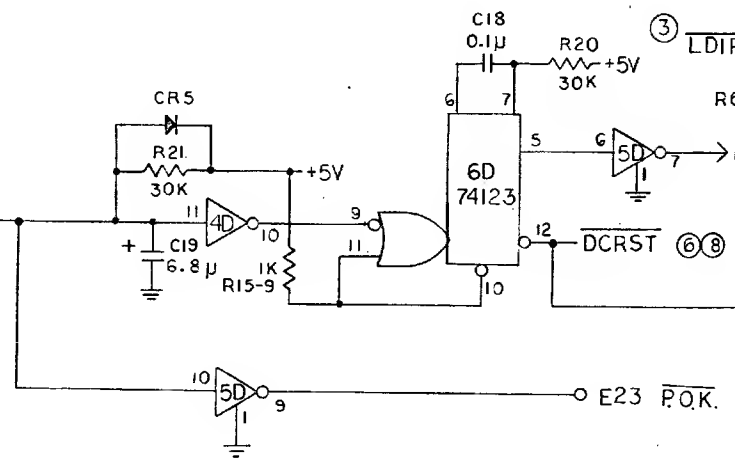


THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.				TOLERANCES					
MATERIAL				DECIMAL	FRAC.	ANG.			
FINISH				XXX ± .01	XXX ± .005	XXX ± .001			
PART NUMBER				DRN T. R. R. 02	CHK T. R. R. 02	ENGR	PROJ	SCALE	UNIT
NEXT ASSEMBLY				COMPUTERVISION CORP.	SOUTH AVENUE	BURLINGTON, MASS. 01803			
QTY									
SIGNATURE									
DATE									
REMOVE ALL BURRS AND SHARP EDGES									
SEE SHT 1									
REVISION DESCRIPTION									
APPRO DATE									
TITLE									
SCHEMATIC DIAGRAM									
CV. PROCESSOR									
COMPUTERVISION CORP.									
SOUTH AVENUE									
BURLINGTON, MASS. 01803									
DWG NO.									
DS2IEI22									
SHEET 3 of 10 SHEETS									

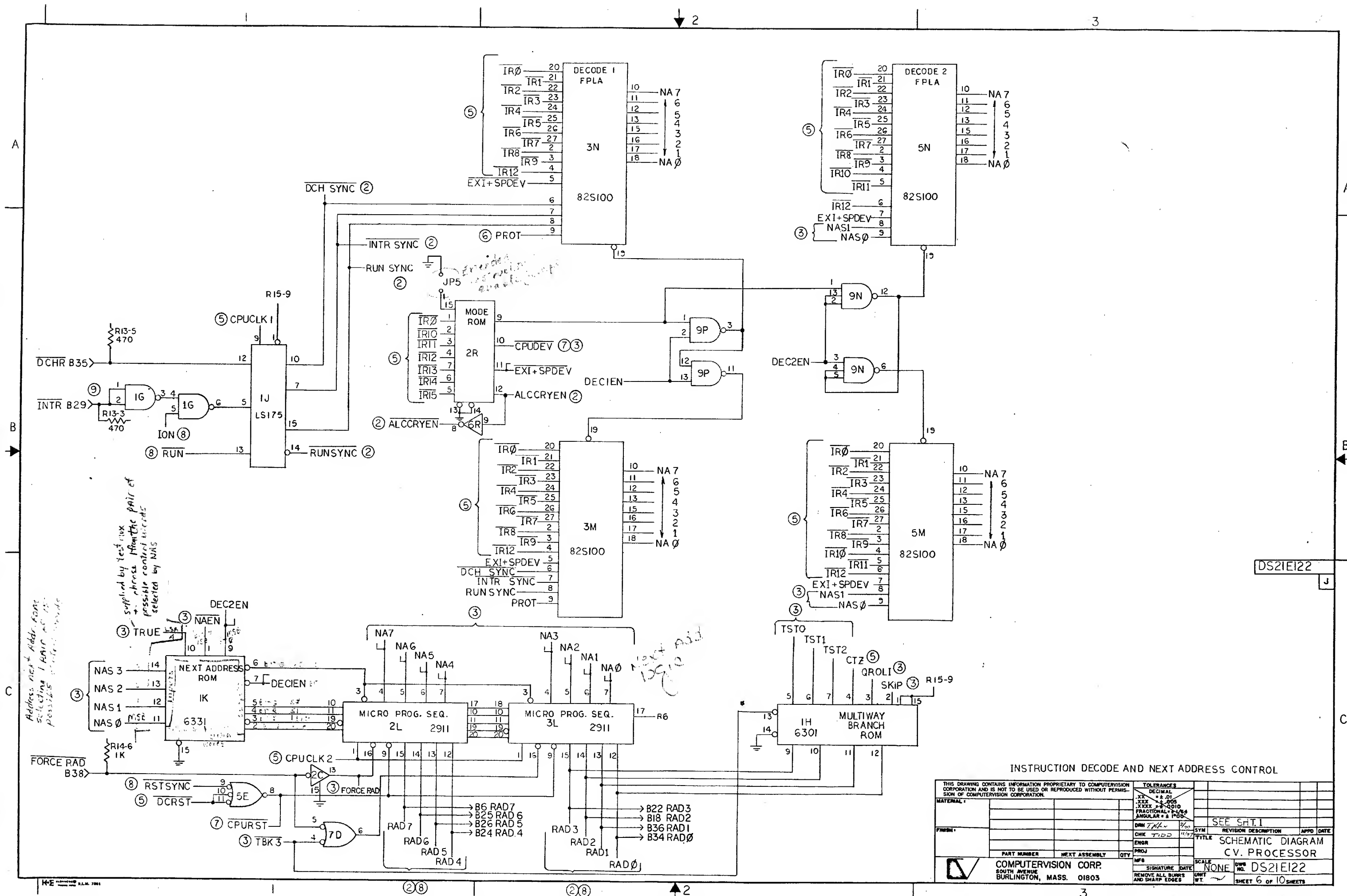


P.O.K. power of

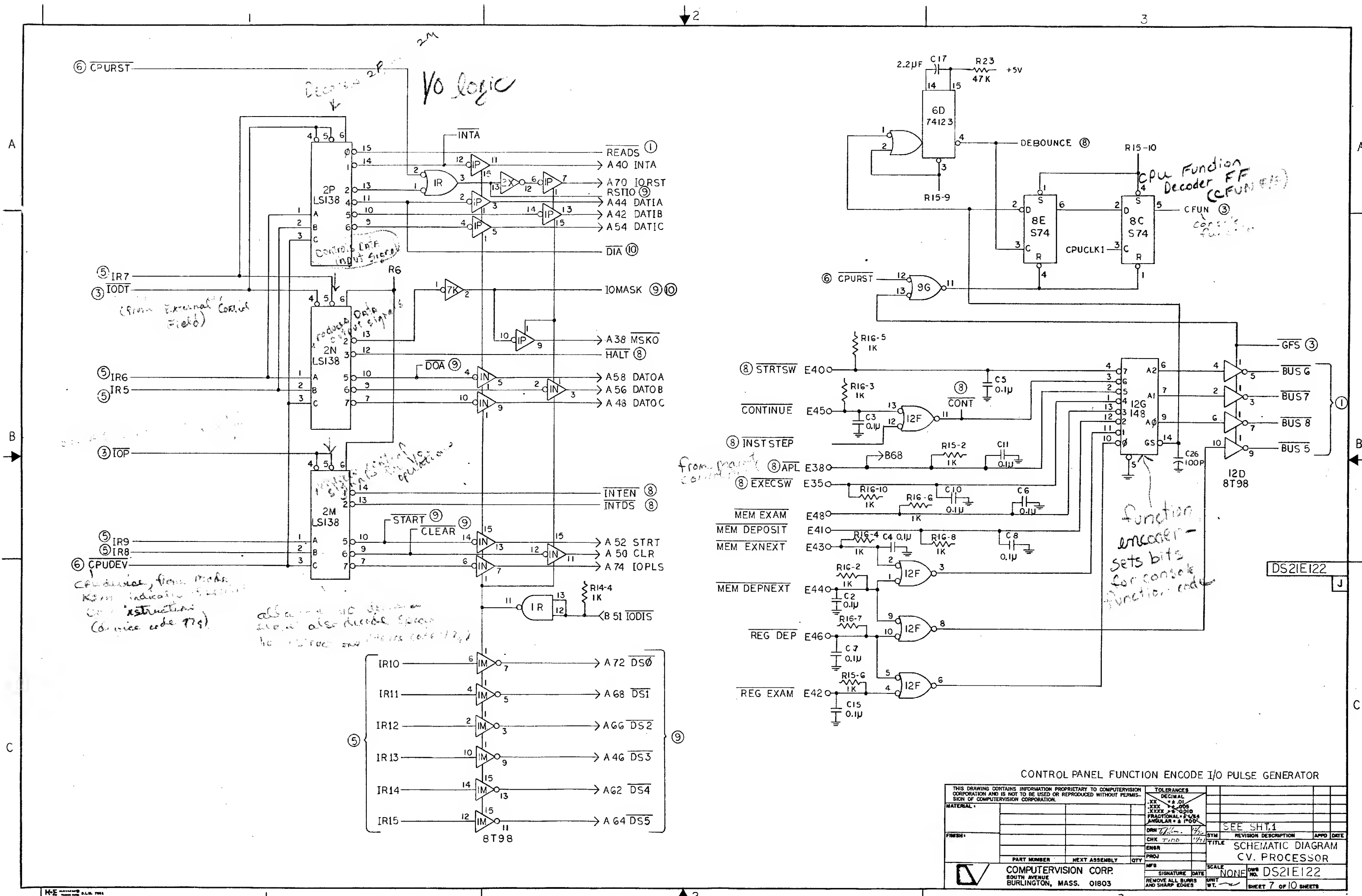
B 90



INSTRUCTION REGISTER, TIMING GENERATOR			
THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.			
TOLERANCES		DECIMAL	
.XX		±.01	
.XXX		±.005	
.XXXX		±.0010	
FRACTIONAL		±.0005	
ANGULAR		±.0005	
MATERIAL		SEE SHT. 1	
FINISH		SYN	
PART NUMBER		REVISION DESCRIPTION	
NEXT ASSEMBLY		APPRO DATE	
QTY		TITLE	
PROJ		SCHEMATIC DIAGRAM	
MFG		CV. PROCESSOR	
SIGNATURE		SCALE	
DATE		NONE	
REMOVE ALL BURRS AND SHARP EDGES		UNIT	
W.T.		NO. DS2IE122	
SHEET 5 OF 10 SHEETS			

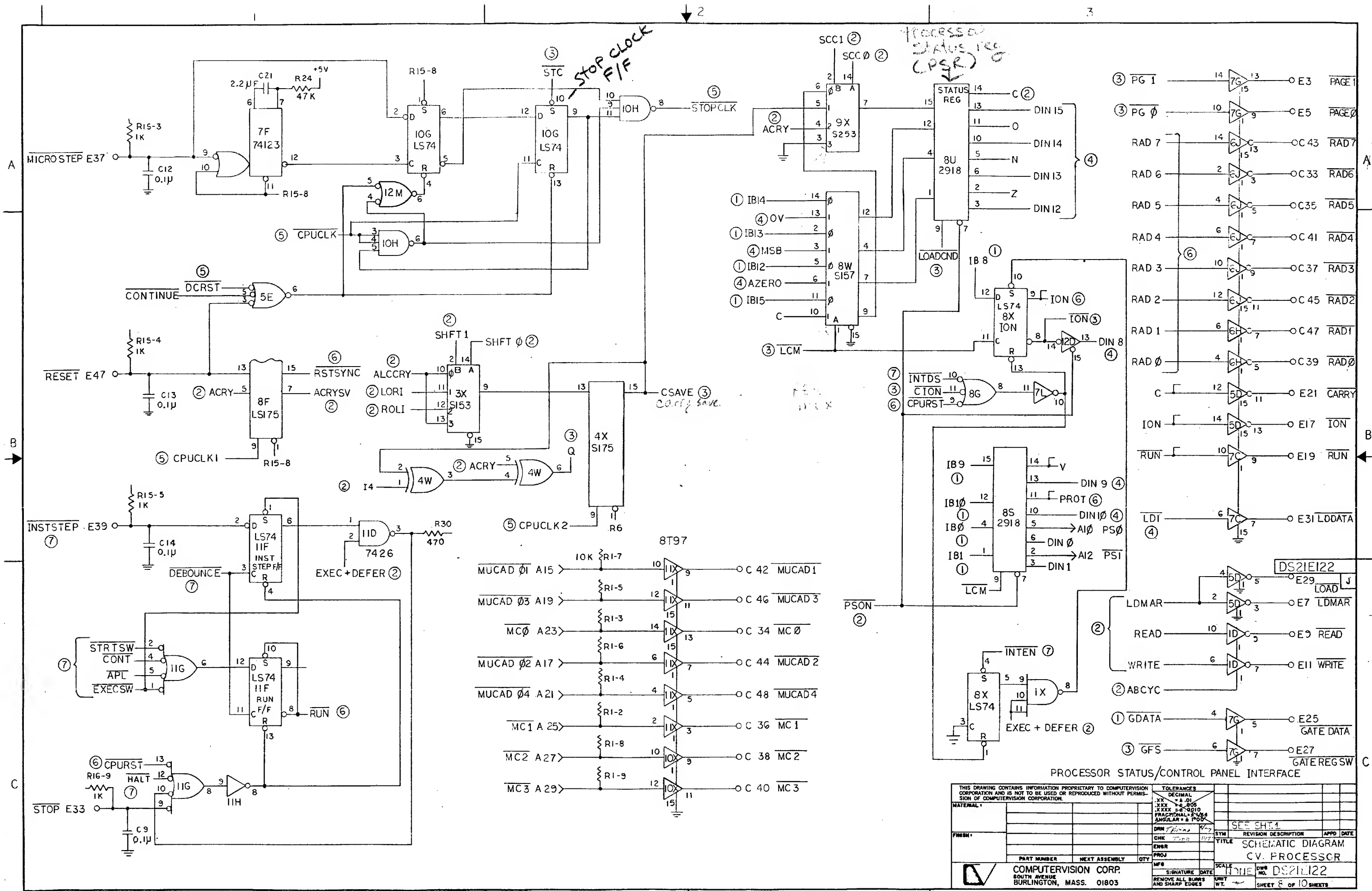


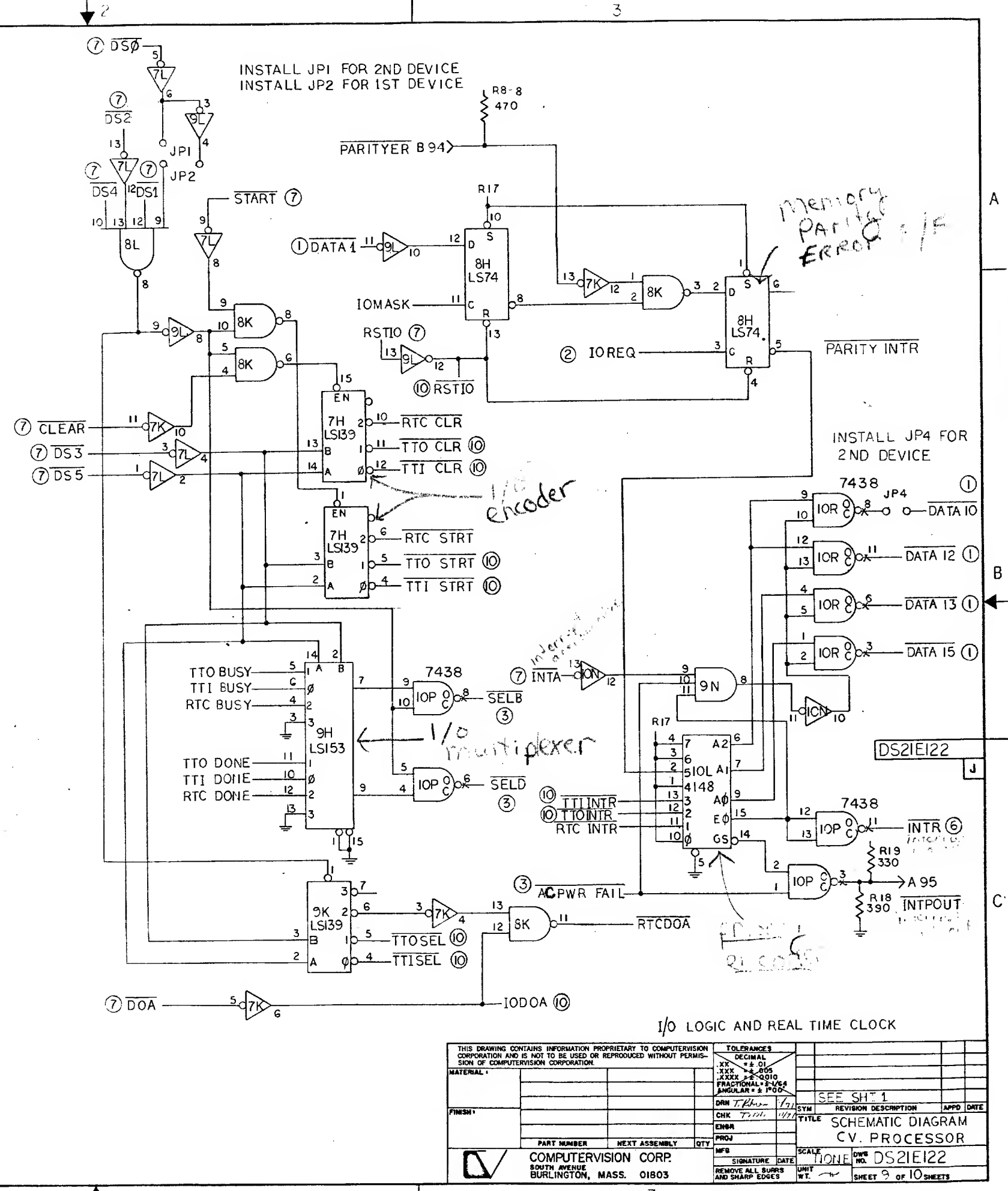
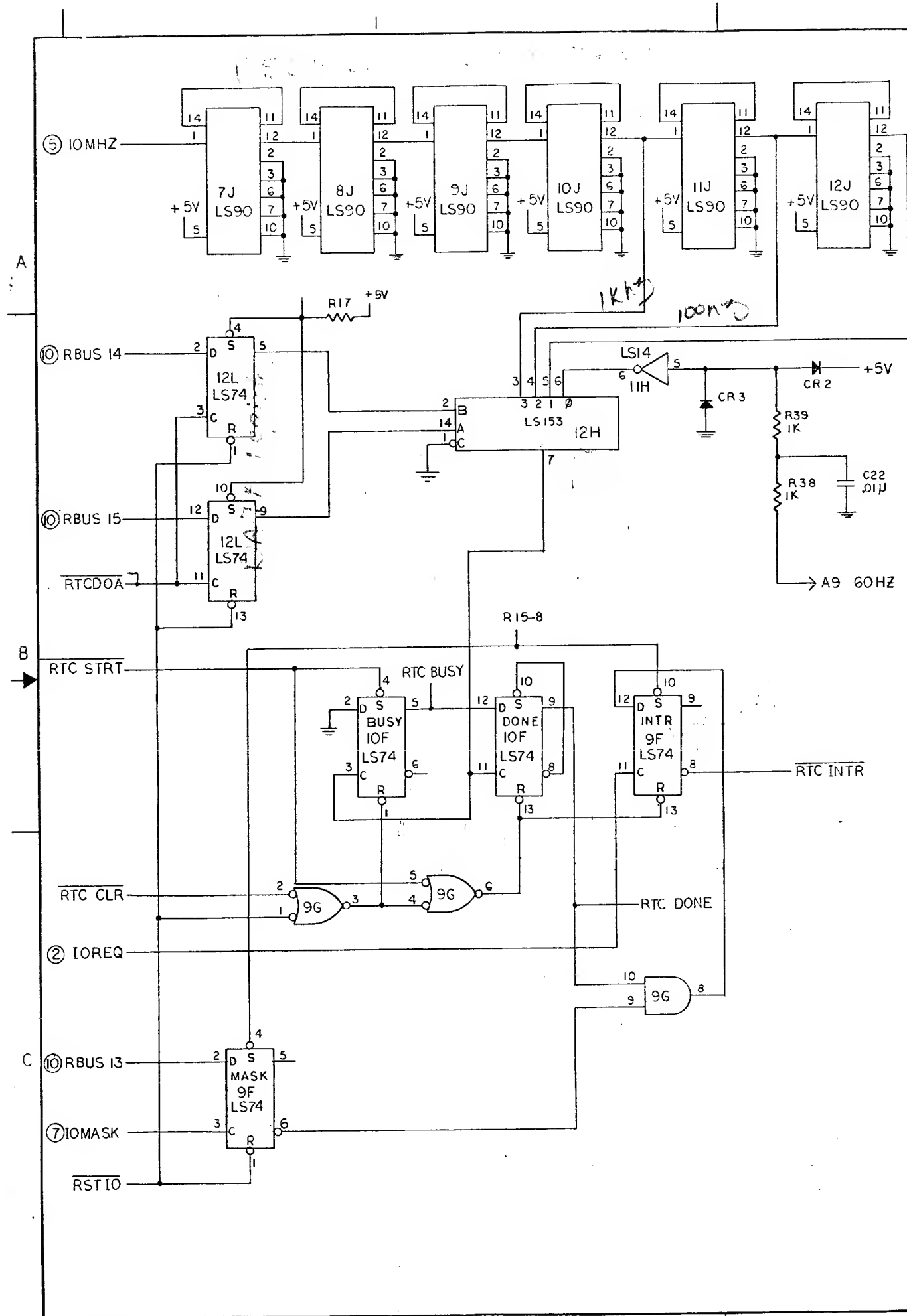
INSTRUCTION DECODE AND NEXT ADDRESS CONTROL			
THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.			
TOLERANCES		DECIMAL	
XX = ± .01		XXX = ± .005	
XXXX = ± .0010		FRACTIONAL = ± .0004	
ANGULAR = ± 1° 00'			
MATERIAL:		SEE SHT. 1	
FINISH:		SYN REVISION DESCRIPTION APPD DATE	
PART NUMBER		TITLE	
NEXT ASSEMBLY		CV. PROCESSOR	
QTY		SCALE	
NFS		NONE	
SIGNATURE		DATE	
REMOVE ALL BURNS AND SHARP EDGES		UNIT	
COMPUTERVISION CORP.		DWS NO. DS21E122	
SOUTH AVENUE		SHEET 6 OF 10 SHEETS	
BURLINGTON, MASS. 01803			

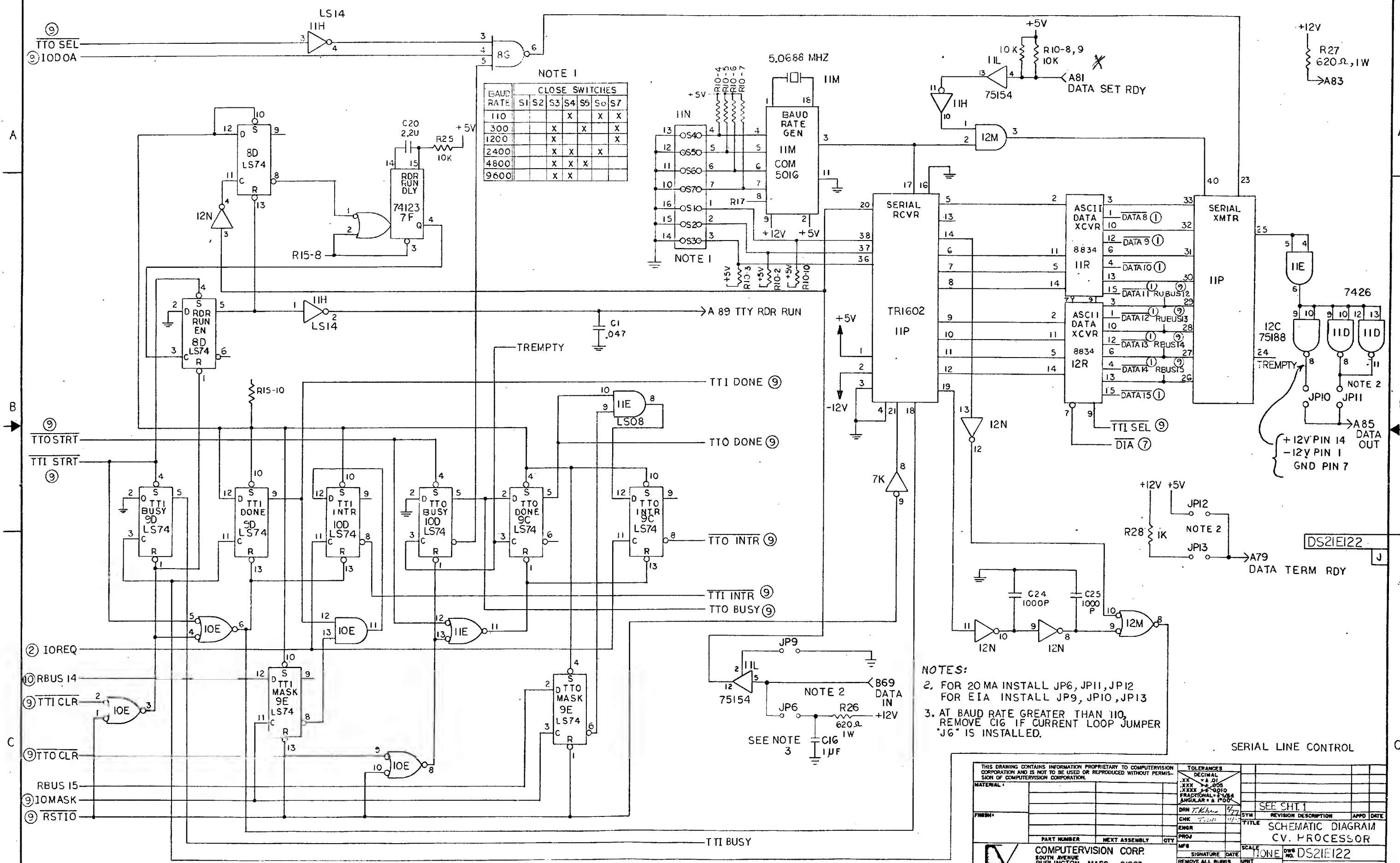


CONTROL PANEL FUNCTION ENCODE I/O PULSE GENERATOR

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.				TOLERANCES DECIMAL XX ± .01 XXX ± .005 XXXX ± .0010 FRACTIONAL ± 1/16 ANGULAR ± 1°			
MATERIAL:				DRN	1/12	SYN	SEE SHT. 1
FINISH:				CHK	1/12	REVISION DESCRIPTION	APPRO DATE
				ENGR		TITLE	SCHEMATIC DIAGRAM
				PROJ		CV. PROCESSOR	
PART NUMBER	NEXT ASSEMBLY	QTY	PROJ	DATE	SCALE	DWG NO.	DS2IE122
COMPUTERVISION CORP. SOUTH AVENUE BURLINGTON, MASS. 01803				SIGNATURE	DATE	UNIT	WT.
REMOVE ALL BURRS AND SHARP EDGES				SHEET 7 OF 10 SHEETS			

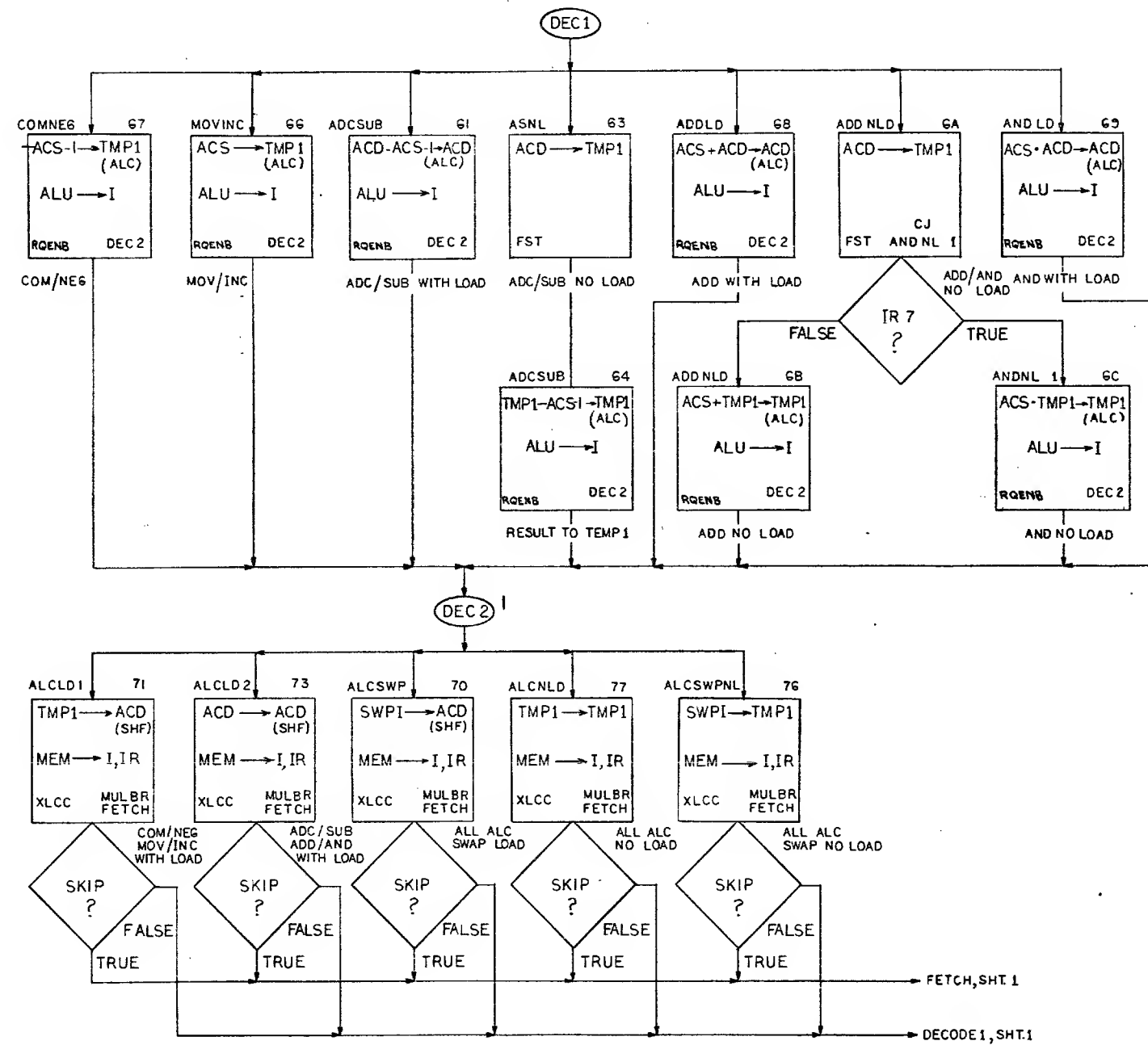






Microprogram Flow Chart

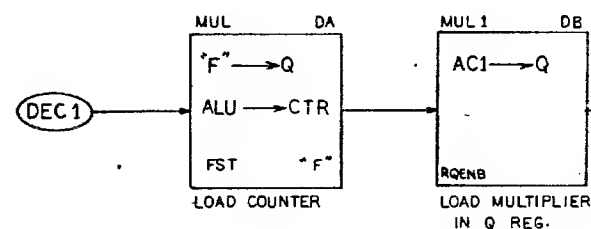
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DS21E015
E

ALC INSTRUCTIONS

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.				TOLERANCES DECIMAL .XX ±.005 .XXX ±.001 FRACTIONAL ANGULAR ±.5 DEG		SEE SHT.1	
MATERIAL		FINISH		CHK		TITLE CVP MICROPROGRAM FLOW CHARTS	
PART NUMBER		NEXT ASSEMBLY		QTY		REV. NO. DS21E015	
COMPUTERVISION CORP. SOUTH AVENUE BURLINGTON, MASS. 01803				SIGNATURE DATE		SCALE NONE	
REMOVE ALL BOWS AND SHARP EDGES				UNIT		SHEET 3 OF 27 SHEETS	



INPUT:

AC2 = MULTIPLICAND

AC1 = MULTIPLIER

AC0 = ADDITIVE CONSTANT

OUTPUT:

AC2 = UNCHANGED

AC1 = LOW ORDER WORD OF $AC0 + (AC1 * AC2)$

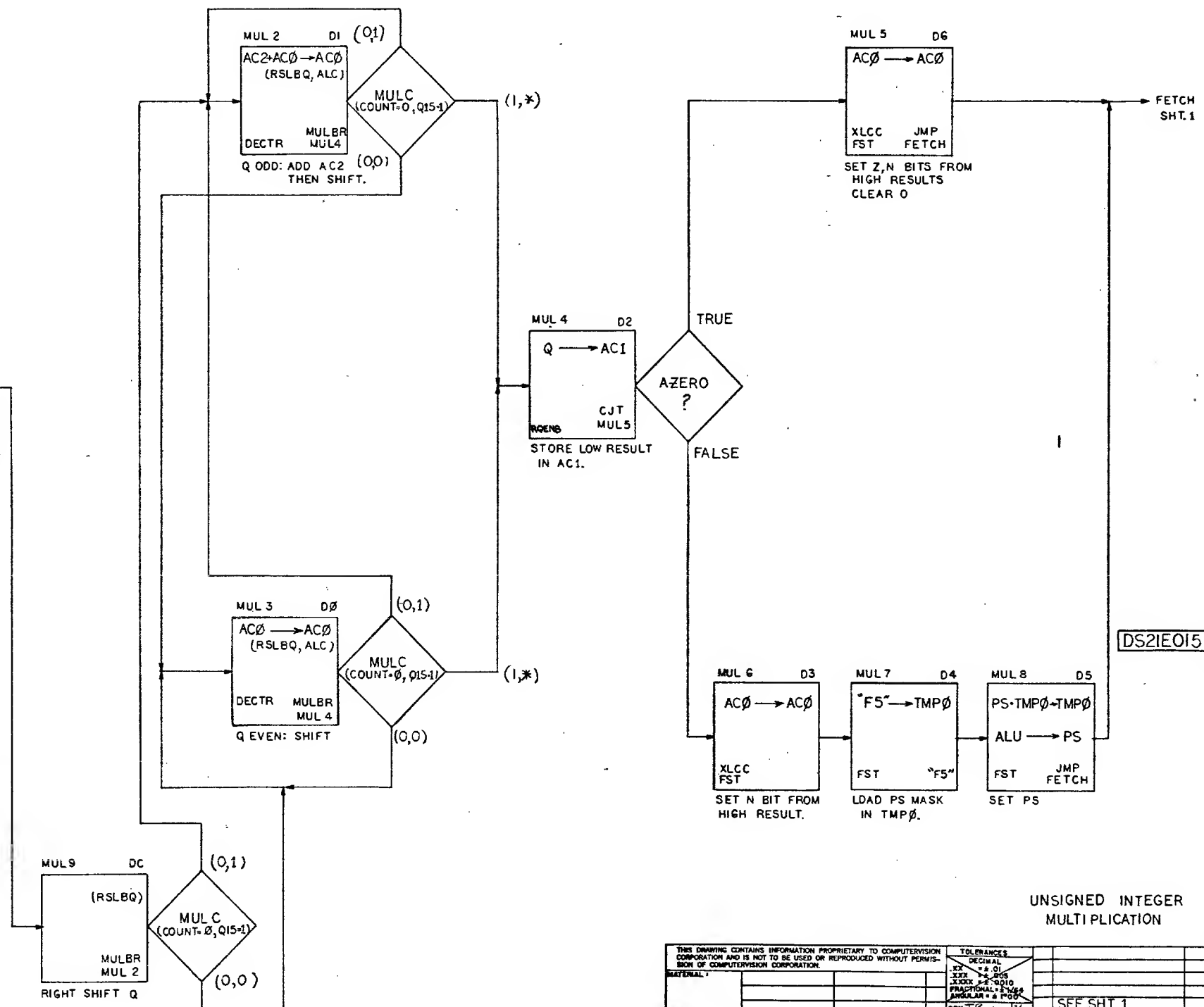
AC0 = HIGH ORDER WORD OF $AC0 + (AC1 * AC2)$

ZBIT = $((AC1 \text{ EQ } 0) \text{ AND } (AC0 \text{ EQ } 0))$

N = MSB OF AC0

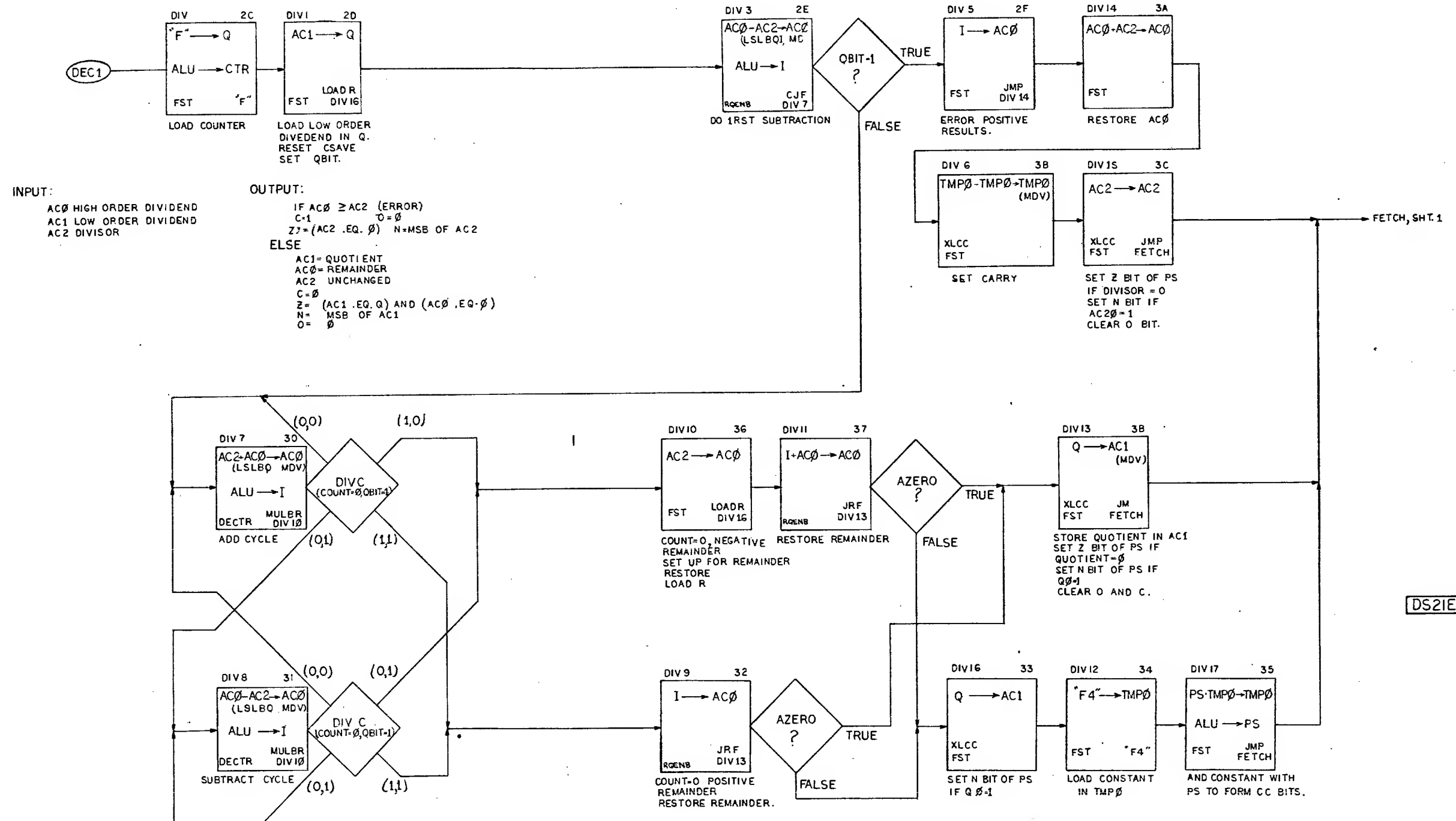
C = NO CHANGE

O = 0



UNSIGNED INTEGER MULTIPLICATION

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.				TOLERANCES DECIMAL XXX ± .01 XXX ± .005 XXX ± .001 FRACTIONAL ± .005 ANGULAR ± .005				SYN	
REVISION				REVISION				SYN	
PART NUMBER				NEXT ASSEMBLY				QTY	
COMPUTERVISION CORP. SOUTH AVENUE BURLINGTON, MASS. 01803				SIGNATURE DATE				SCALE NONE	
DRAWN BY				CHECKED BY				DATE	
DESIGNED BY				APPROVED BY				DATE	
PROJECT				TITLE				CVP MICROPROGRAM FLOW CHARTS	
DRAWING NO. DS21E015				SHEET 4 OF 27 SHEETS					

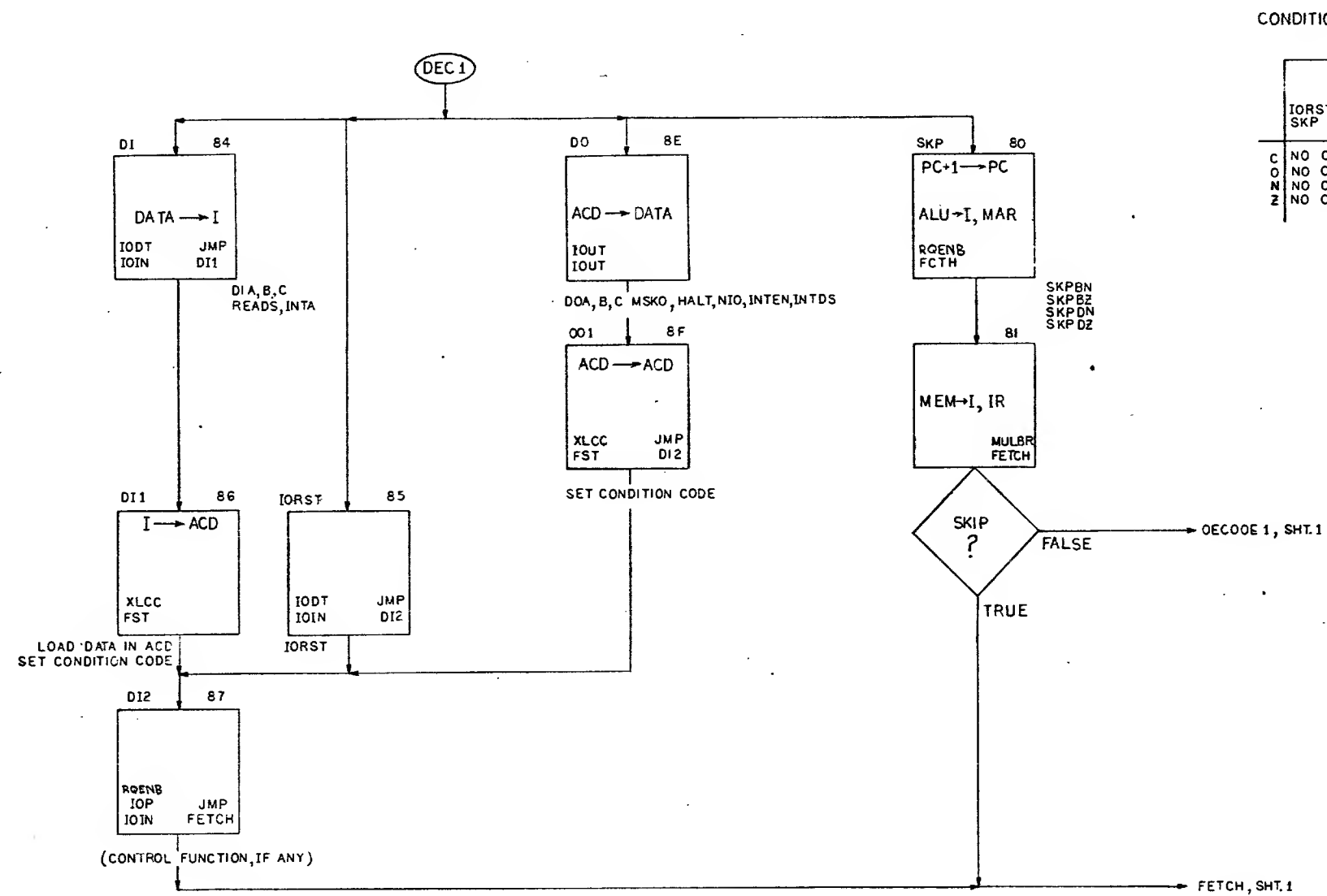


DS21E015

E

UNSIGNED INTEGER DIVISION

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.				TOLERANCES DECIMAL XXX ± .01 XXX ± .005 FRACTIONS ± 1/64 ANGULAR ± 1° 00'	
MATERIAL				SYN	REVISION DESCRIPTION
FRESH				CHK	
				ENGR	
				PROJ	
PART NUMBER	NEXT ASSEMBLY	QTY	INPS	SIGNATURE	DATE
COMPUTERVISION CORP. SOUTH AVENUE BURLINGTON, MASS. 01803			SCALE NONE DWG NO. DS21E015 SHEET 5 OF 27 SHEETS		



CONDITION CODE BITS FOR I/O

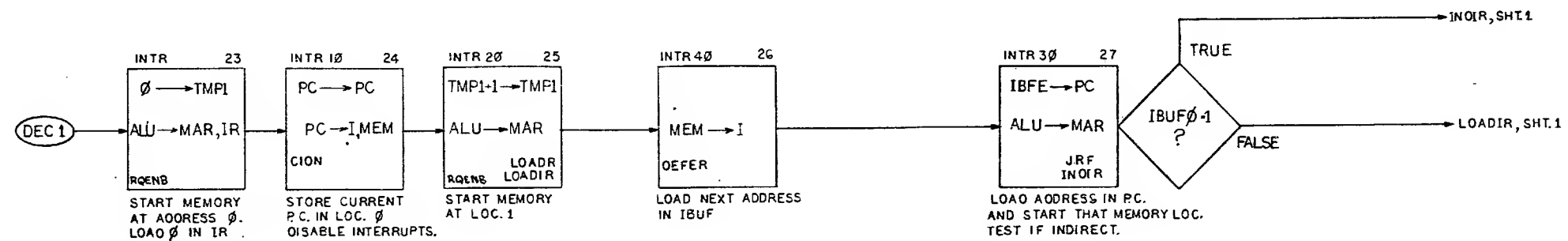
	IORST SKP	OIA, B, C READS, INTA	DOA, B, C MSKO, HALT, NIO, INTEN, INTDS
C	NO CHANGE	NO CHANGE	NO CHANGE
O	NO CHANGE	NO CHANGE	NO CHANGE
N	NO CHANGE	MSB DATA IN	MSB DATA OUT
Z	NO CHANGE	DATA IN = 0	DATA OUT = 0

I/O INSTRUCTIONS

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.		TOLERANCES DECIMAL XX ± .01 XXX ± .005 FRACTIONAL X/XX ± .001 ANGULAR ± .005		DATE 4/77	
MATERIAL		CHK	ENGR	PROJ	SYN
FINISH					
PART NUMBER		NEXT ASSEMBLY	QTY	TITLE CVP MICROPROGRAM FLOW CHART	
COMPUTERVISION CORP. SOUTH AVENUE BURLINGTON, MASS. 01803			SCALE NONE SHEET 5 OF 27		

23521E015

E



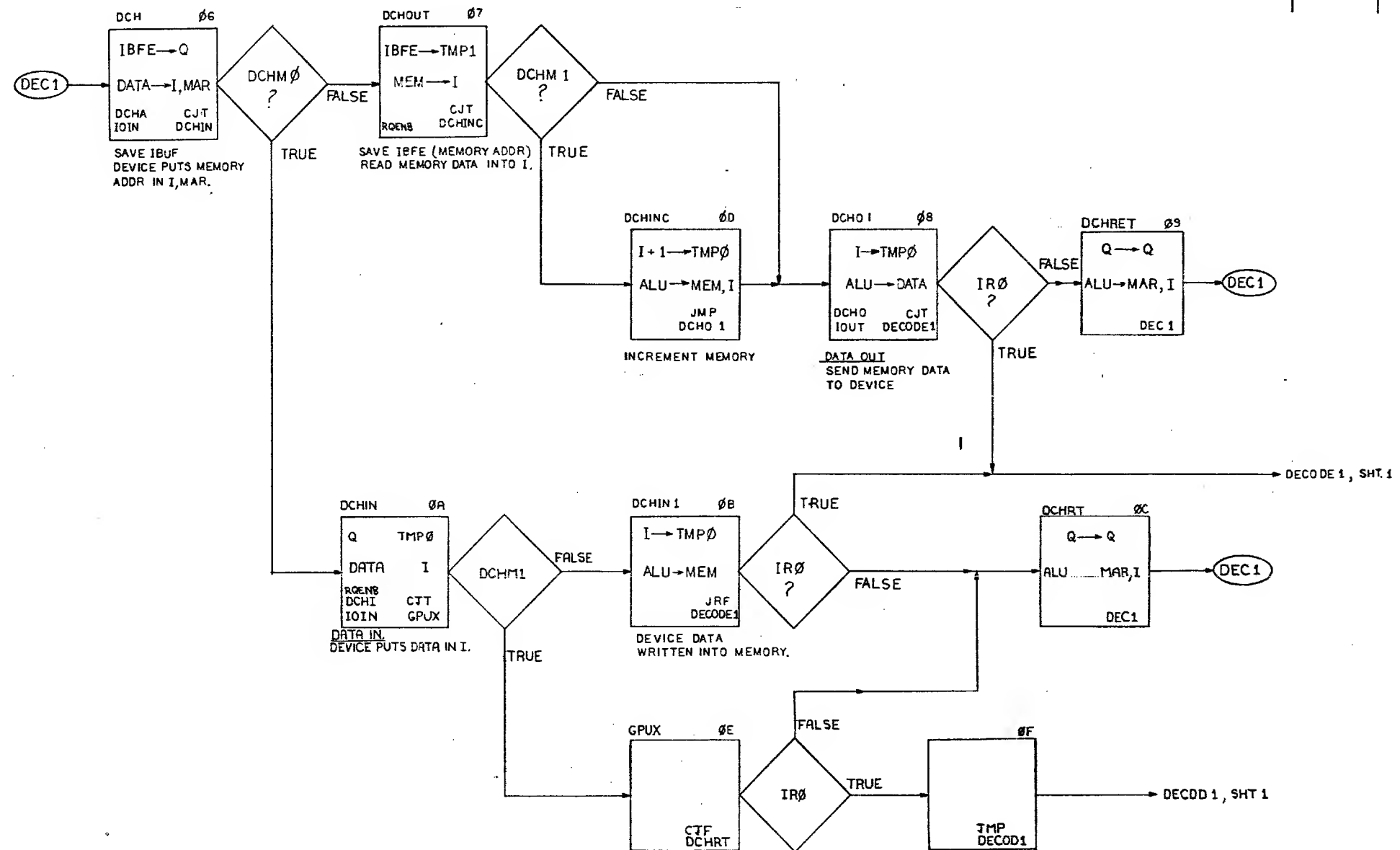
DS21E015

E

INTERRUPT

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISS.		TOLERANCES DECIMAL .XX ± .01 .XXX ± .005 FRACTIONAL ± .004 ANGULAR ± .000"		SYN	
MATERIAL:		DRN T. Kistner 9/77	CHK	ENGR	PROJ
PREP:					
PART NUMBER	NEXT ASSEMBLY	QTY	SCALE	SHEET	NO.
COMPUTERVISION CORP. SOUTH AVENUE BURLINGTON, MASS. 01803			NONE	DS21E015	
REMOVE ALL BURS AND SHARP EDGES		UNIT	WT.	SHEET 7 OF 27 SHEETS	

FUNCTION	DCHM0	DCHM1
DATA OUT	0	0
INCREMENT MEMORY	0	1
DATA IN	1	0
GPU TRANSFER	1	1



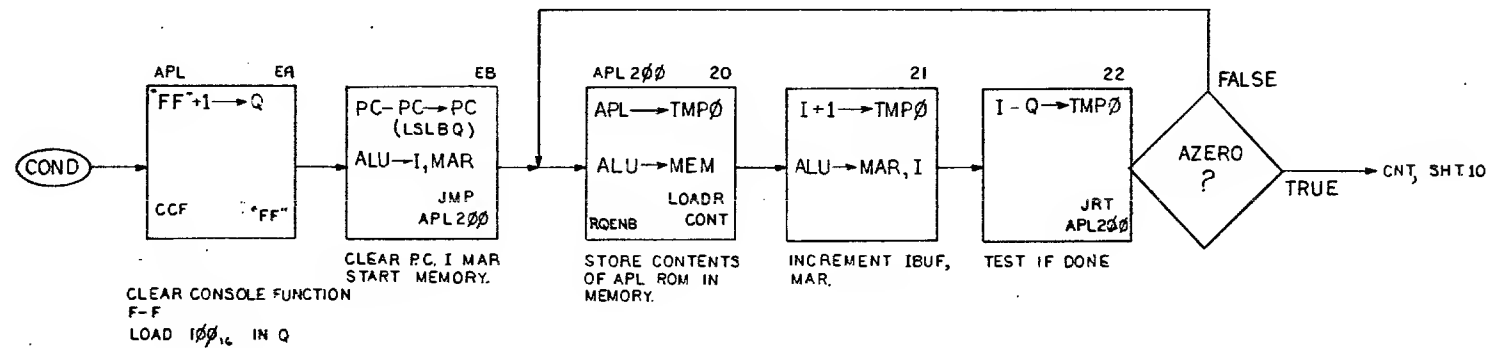
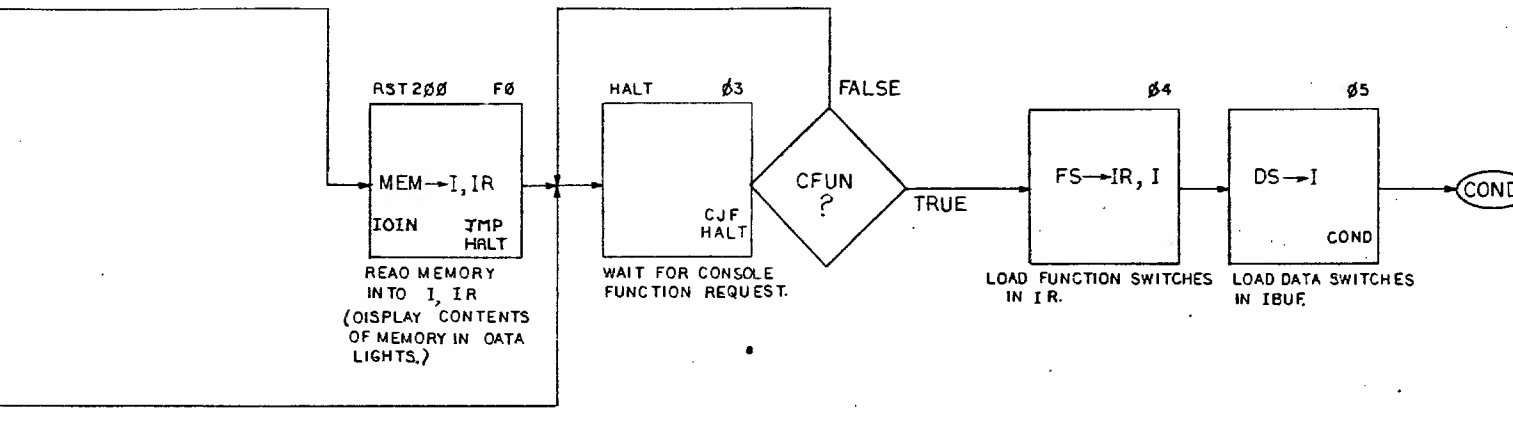
DS2IE015	E
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DATA CHANNEL

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.				TOLERANCES DECIMAL XX .XX XXX .XXX FRACTIONAL = 1/64 ANGULAR = 1/2°			
MATERIAL:				DIN 7.2200 1/2"		SEE SHT.1	
FINISH:				CHK		SYM REVISION DESCRIPTION APPD DATE	
				ENR		TITLE	
				ENR		CVP MICROPROGRAM	
				PROJ		FLOW CHART	
PART NUMBER		NEXT ASSEMBLY		QTY			
COMPUTERVISION CORP. SOUTH AVENUE BURLINGTON, MASS. 01803				INFO		SCALE	
				SIGNATURE DATE		NONE DS2IE015	
				REMOVE ALL BURRS AND SHARP EDGES		UNIT W.T.	
						SHEET 8 OF 27 SHEETS	

EXAM, SHT. 10
EXAMN, SHT. 10
DEP 200, SHT. 10
STOP SHT. 10

REGE, SHT. 10
SHT. 25

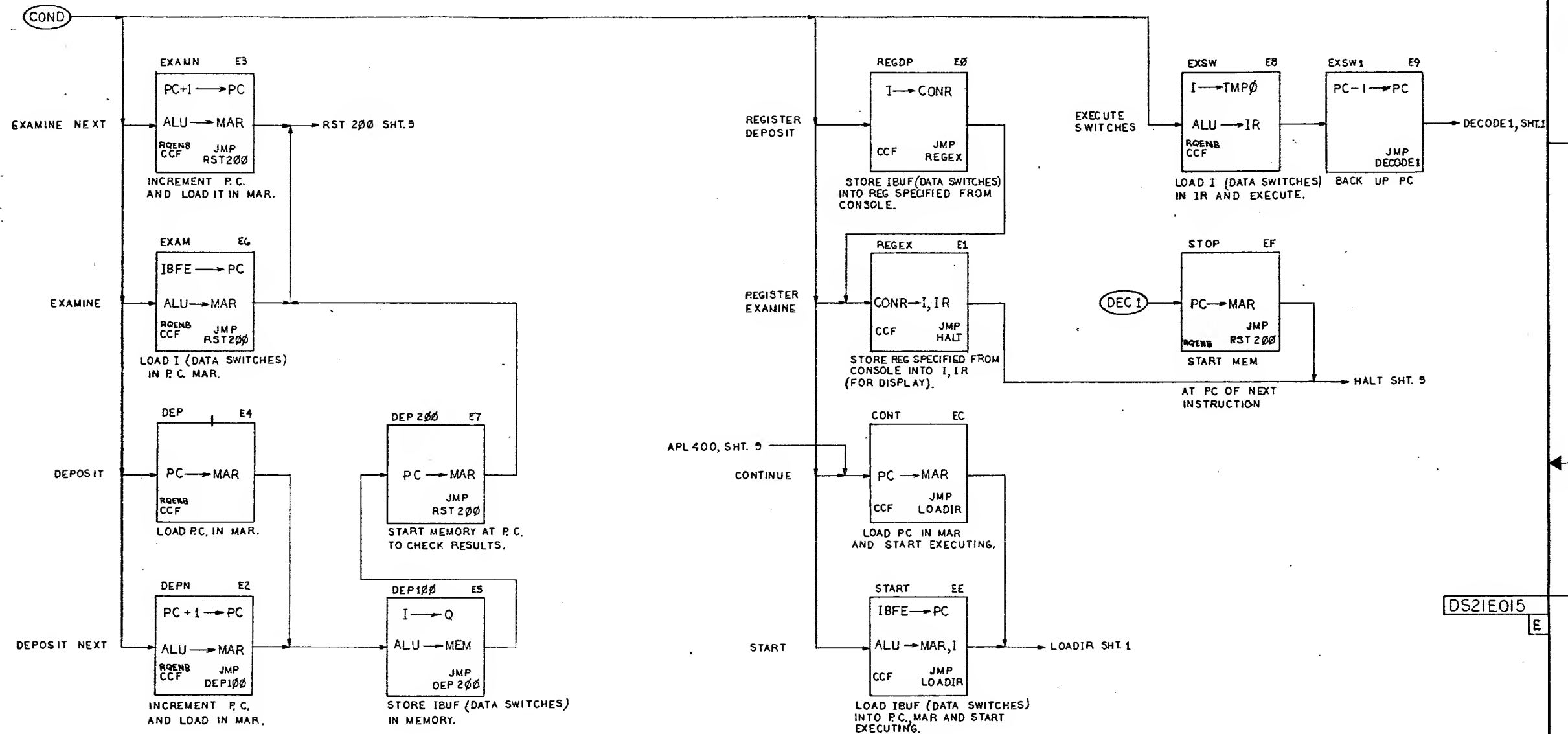


DS2IE015

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CONSOLE FUNCTIONS I
(RESET, HALT STATE, APL)

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MATERIAL	FINISH	DATE	BY	CHK	ENG
DATE	BY	CHK	ENG	PROJ	QTY
PART NUMBER			NEXT ASSEMBLY		
COMPUTERVISION CORP. SOUTH AVENUE BURLINGTON, MASS. 01803			SCALE		
SIGNATURE			DATE		
REMOVE ALL BURNS AND SHARP EDGES			UNIT		
SHEET 9 OF 27			SHEETS		

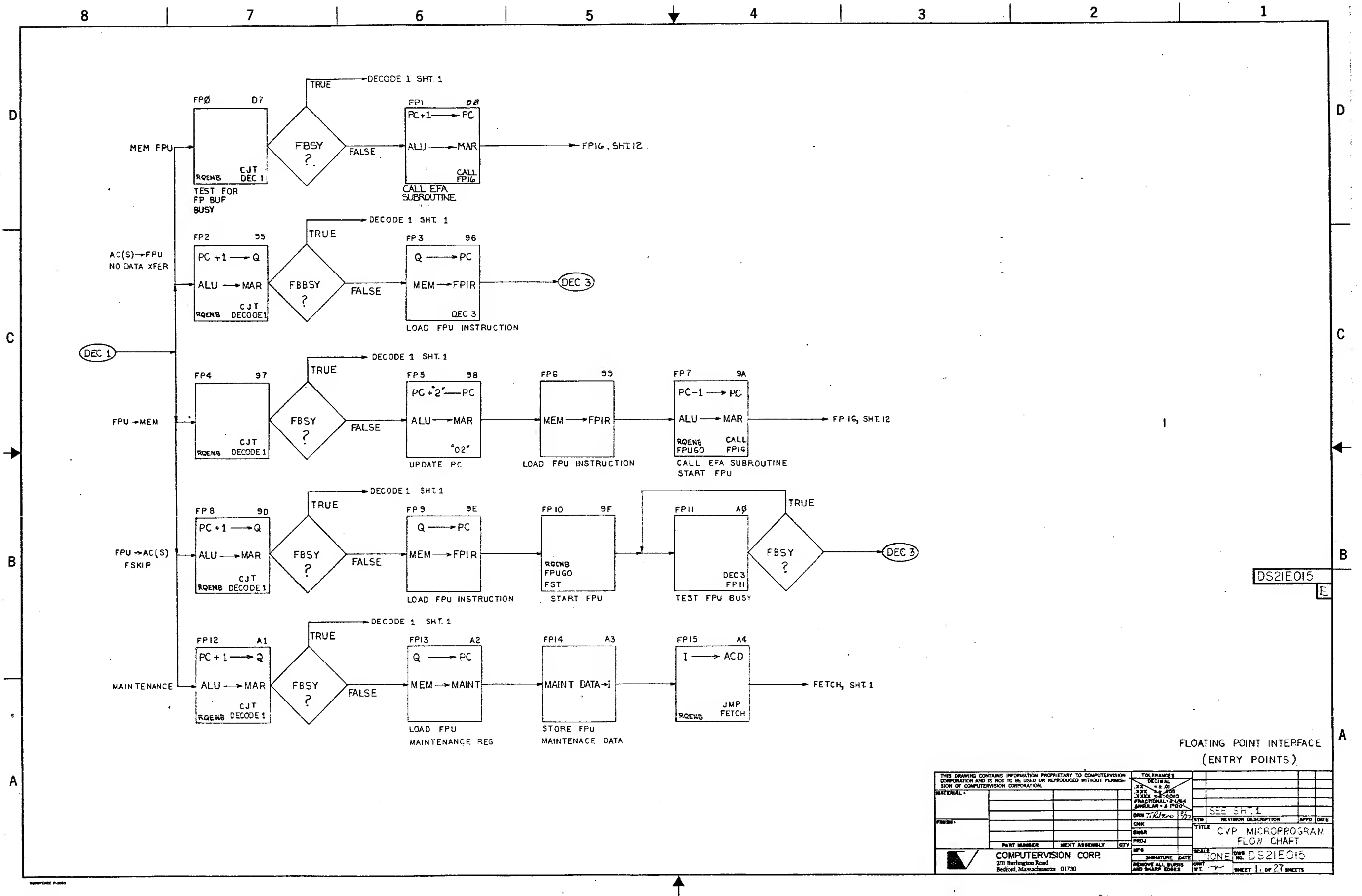


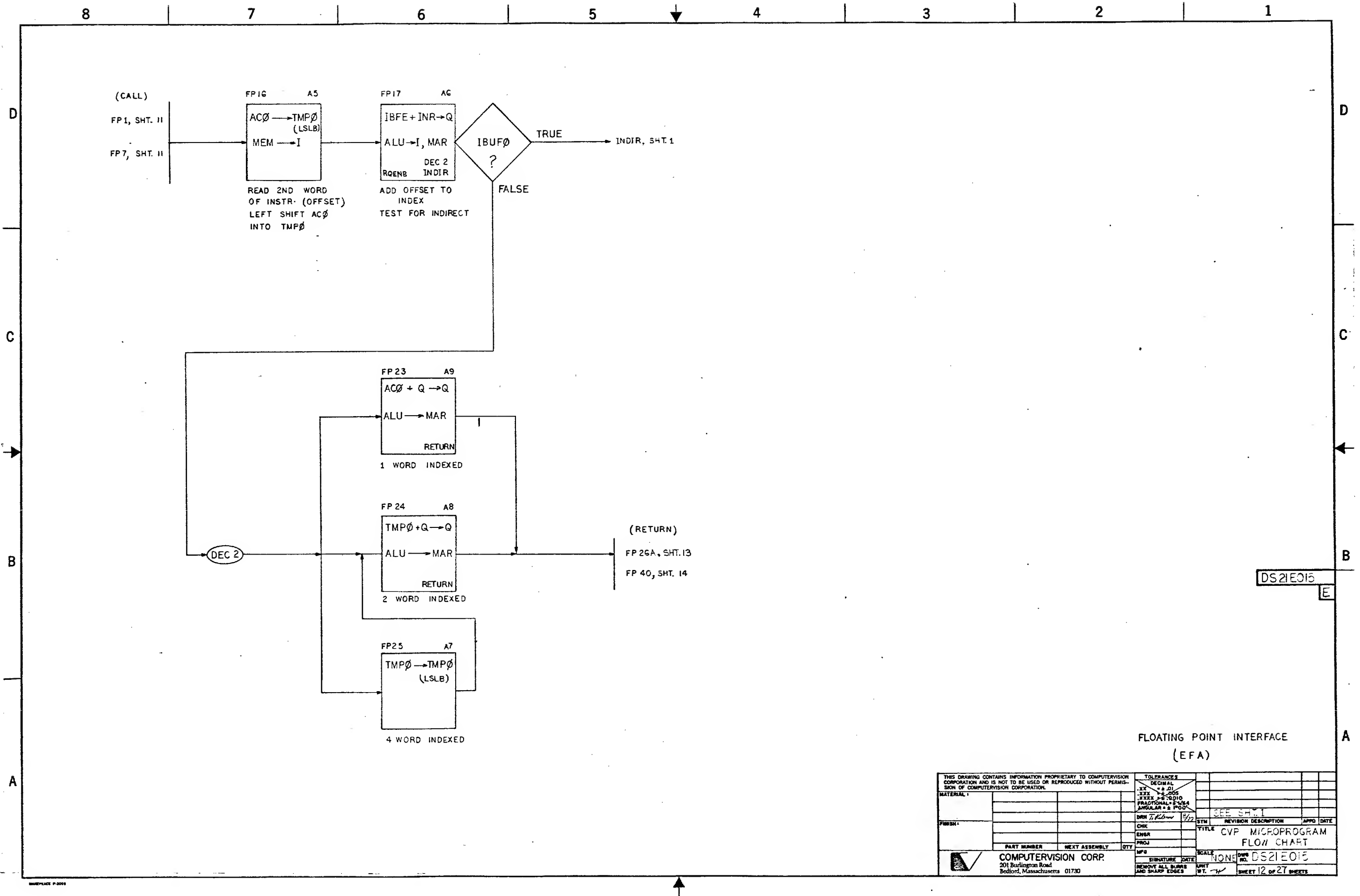
DS21E015

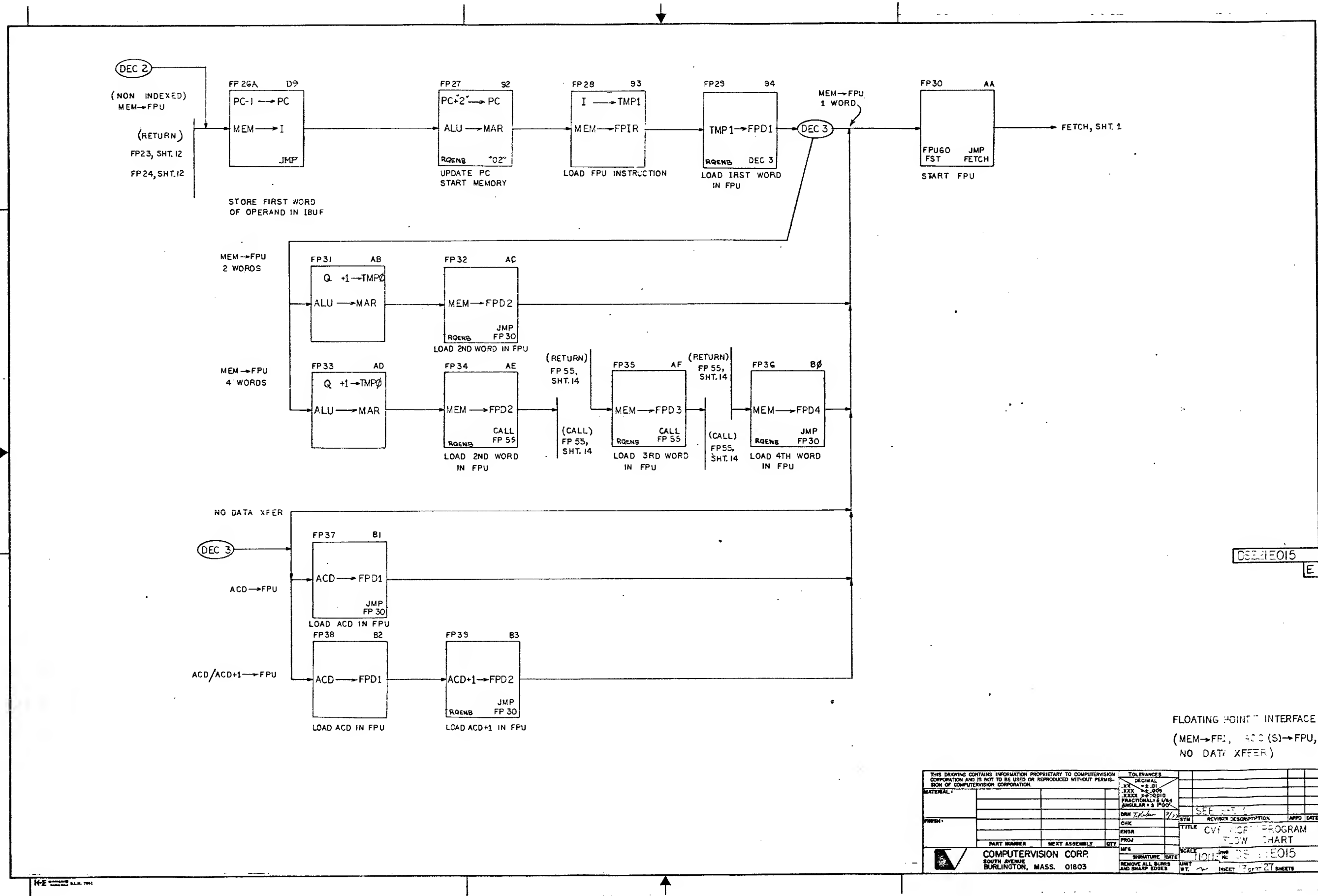
E

CONSOLE FUNCTIONS II

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.		TOLERANCES DECIMAL XXX ± .01 XXX ± .005 XXX ± .0010 FRACTIONAL ± .0064 ANGULAR ± .0001		SYN REV APPD DATE	
MATERIAL		DIM 7.14		SEE SHT. 1	
FINISH		CHK		TITLE	
PART NUMBER		NEXT ASSEMBLY		CVP MICROPROGRAM FLOW CHART	
COMPUTERVISION CORP. SOUTH AVENUE BURLINGTON, MASS. 01803		SCALE NONE		DWG NO. DS21E015	
REMOVE ALL BURRS AND SHARP EDGES		SHEET 10 OF 27 SHEETS			



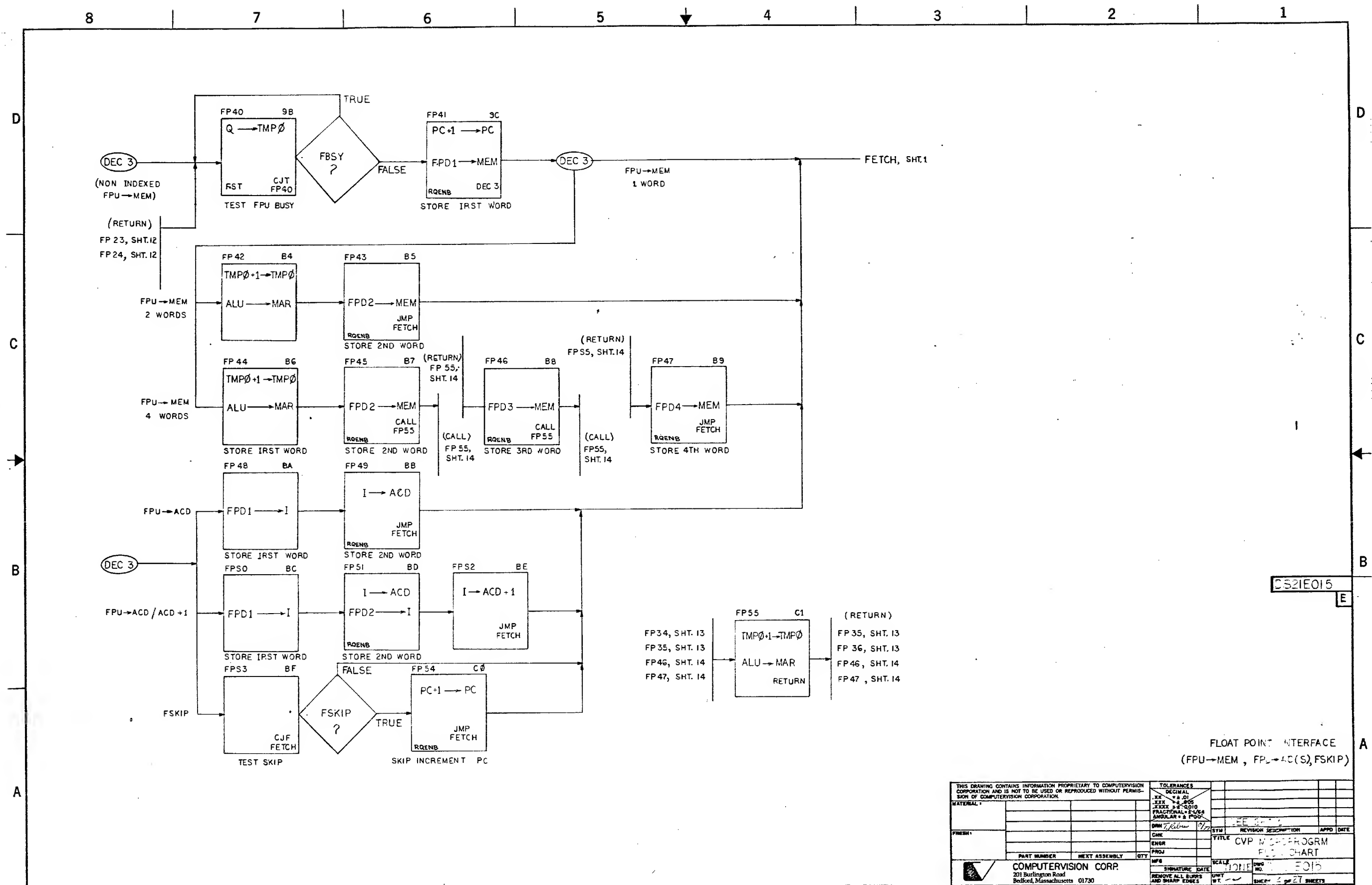


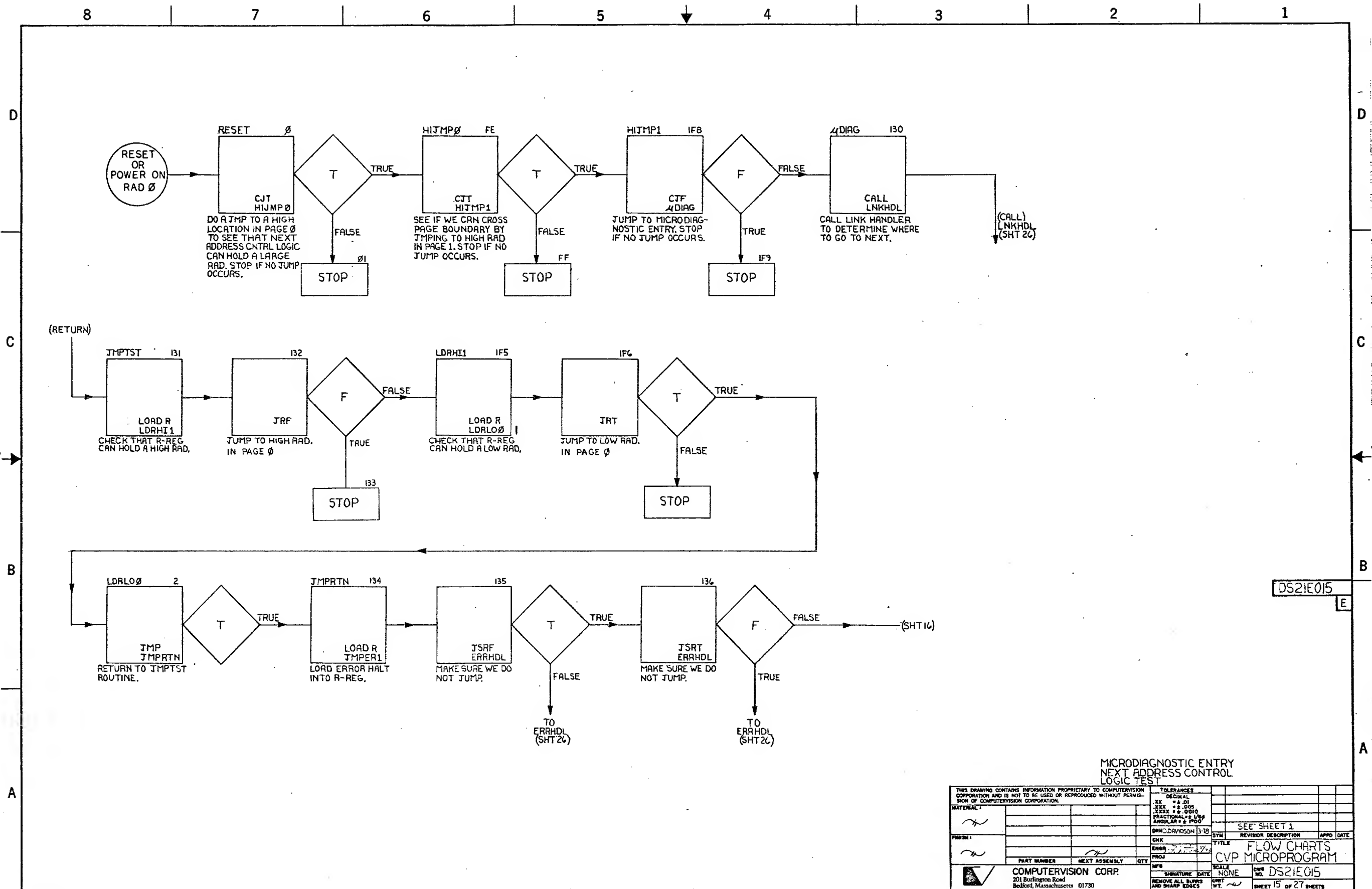


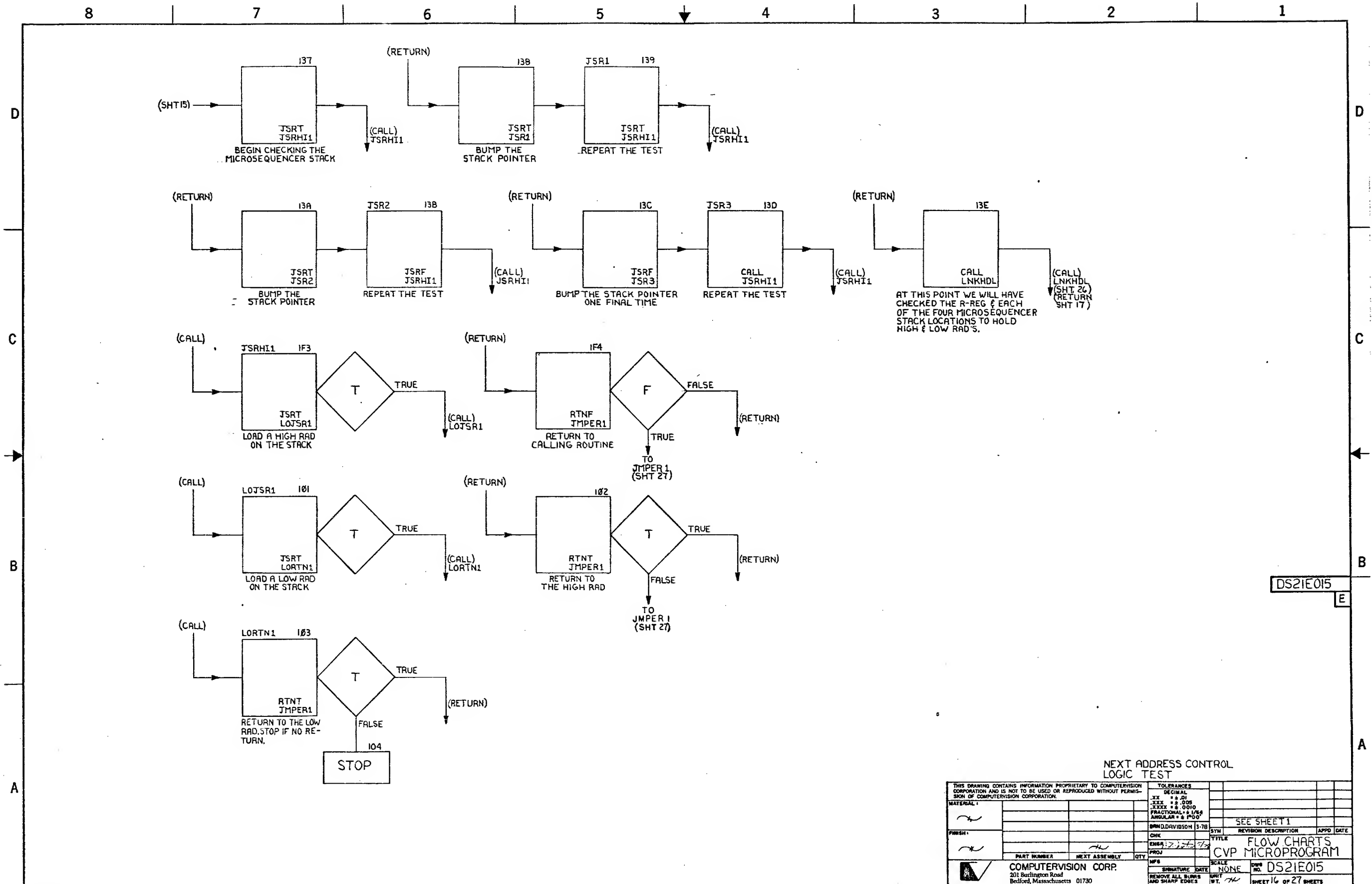
DSERIE015
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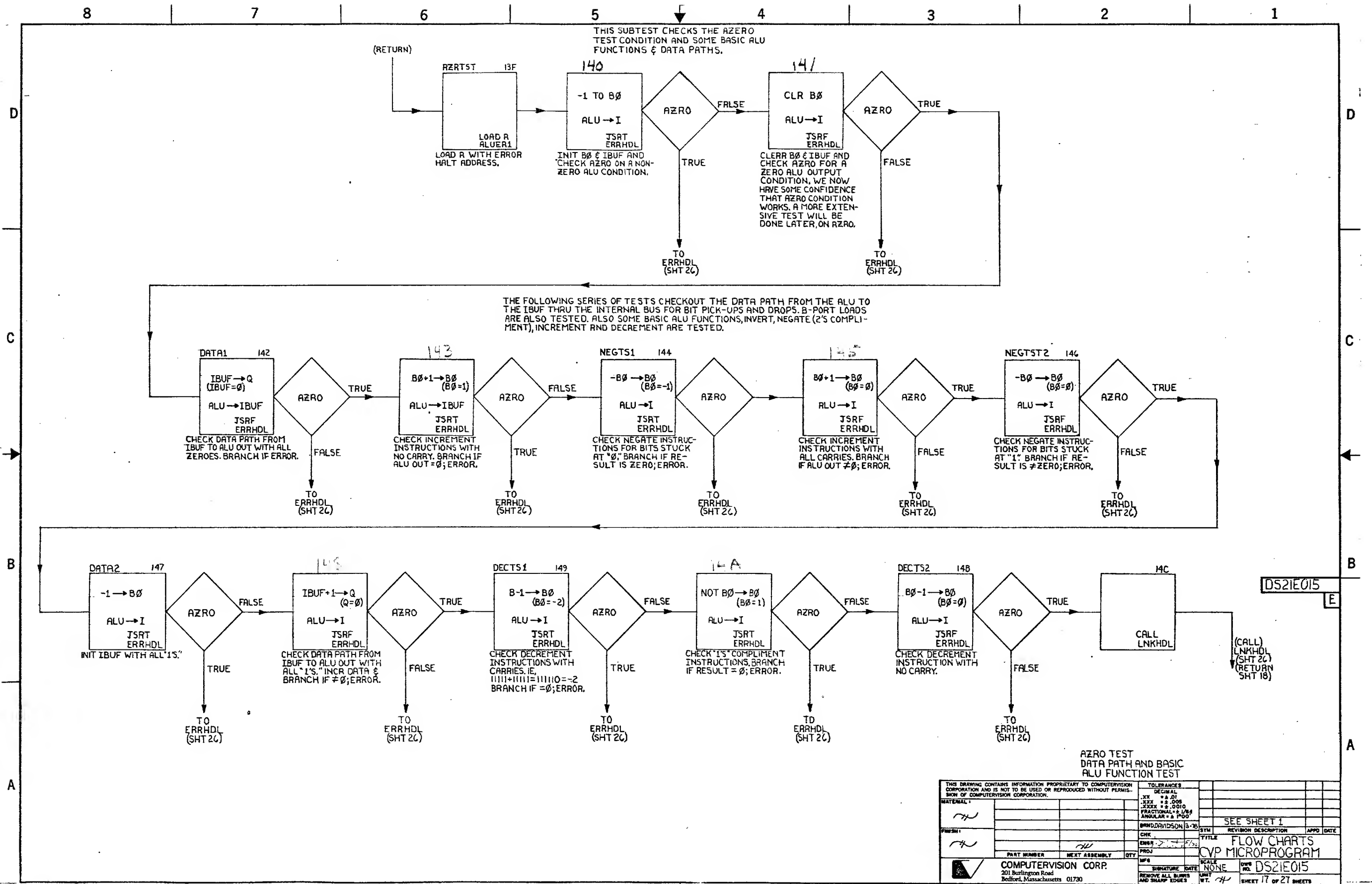
FLOATING POINT INTERFACE
(MEM -> FPU, ADD(S) -> FPU,
NO DATA XFER)

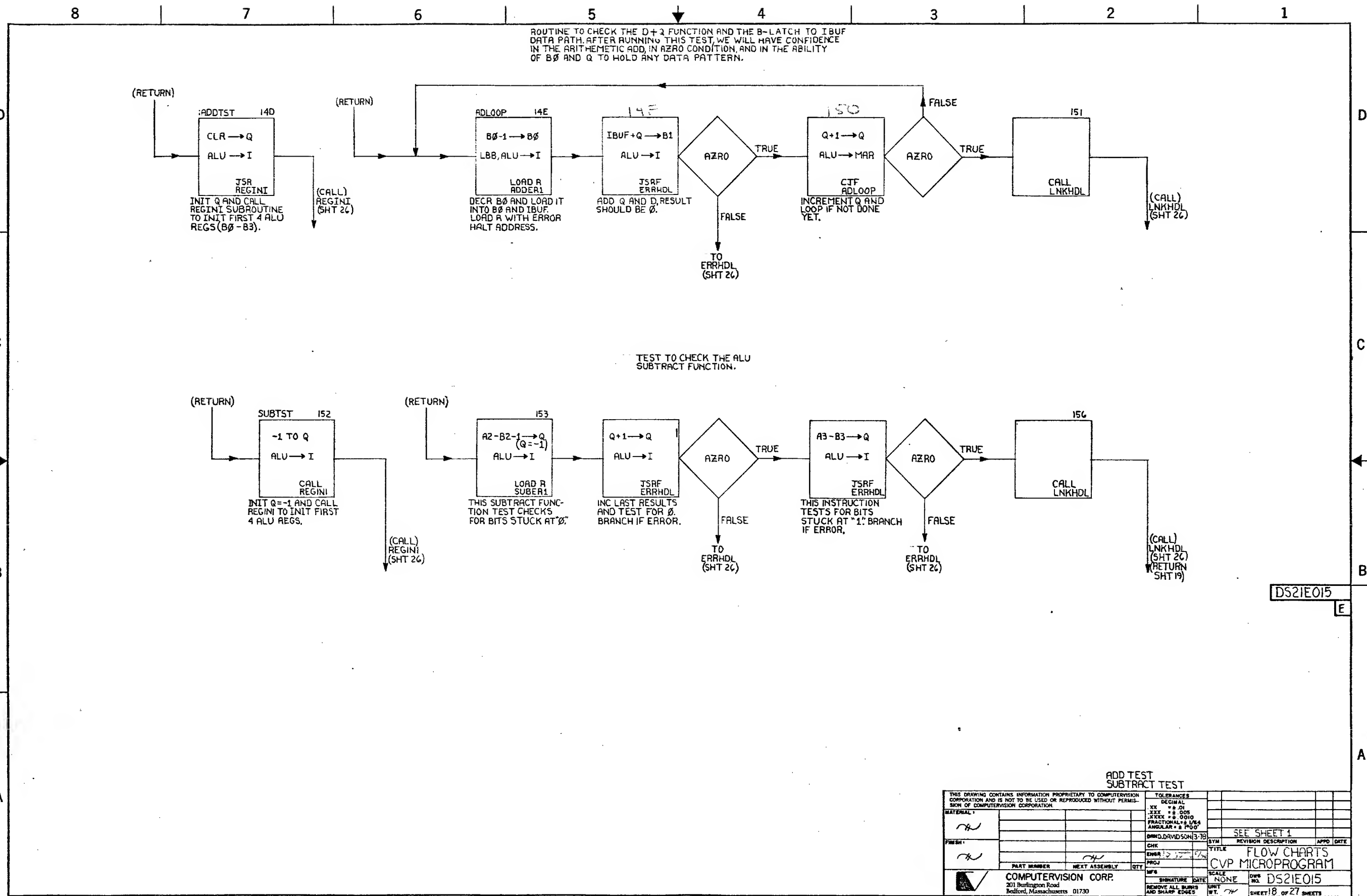
THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.		TOLERANCES DECIMAL .XX = .01 .XXX = .005 FRACTIONALS 1/64 ANGULAR 1/2 DEG		DATE 7/1/80	
MATERIAL		CHK		ENG	
PROJ		PROJ		PROJ	
PART NUMBER		NEXT ASSEMBLY		QTY	
COMPUTERVISION CORP. SOUTH AVENUE BURLINGTON, MASS. 01803			SCALE 1:1		
SIGNATURE DATE			SCALE 1:1		
REMOVE ALL BOMBS AND SHARP EDGES			SHEET 13 OF 27 SHEETS		

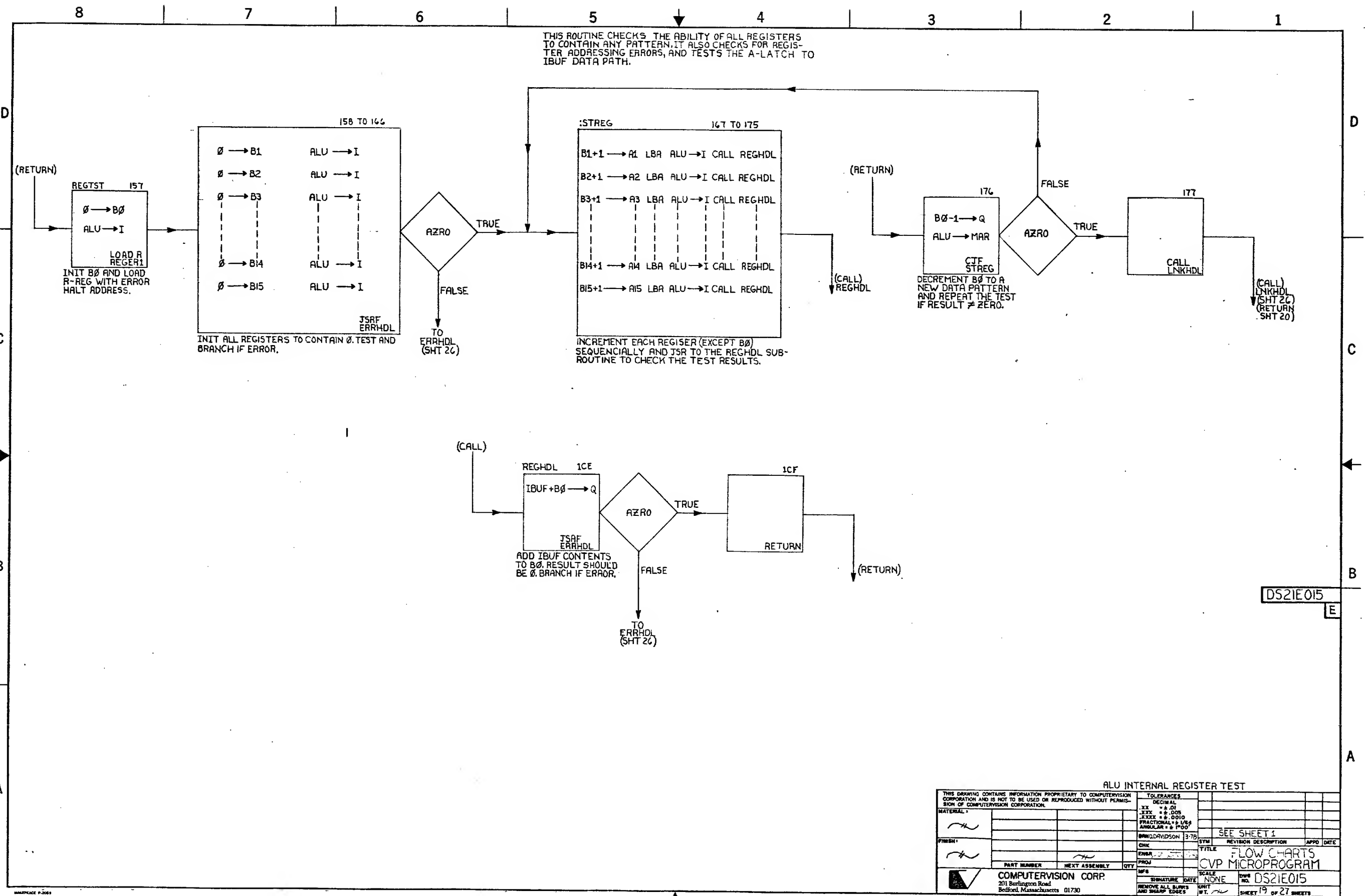


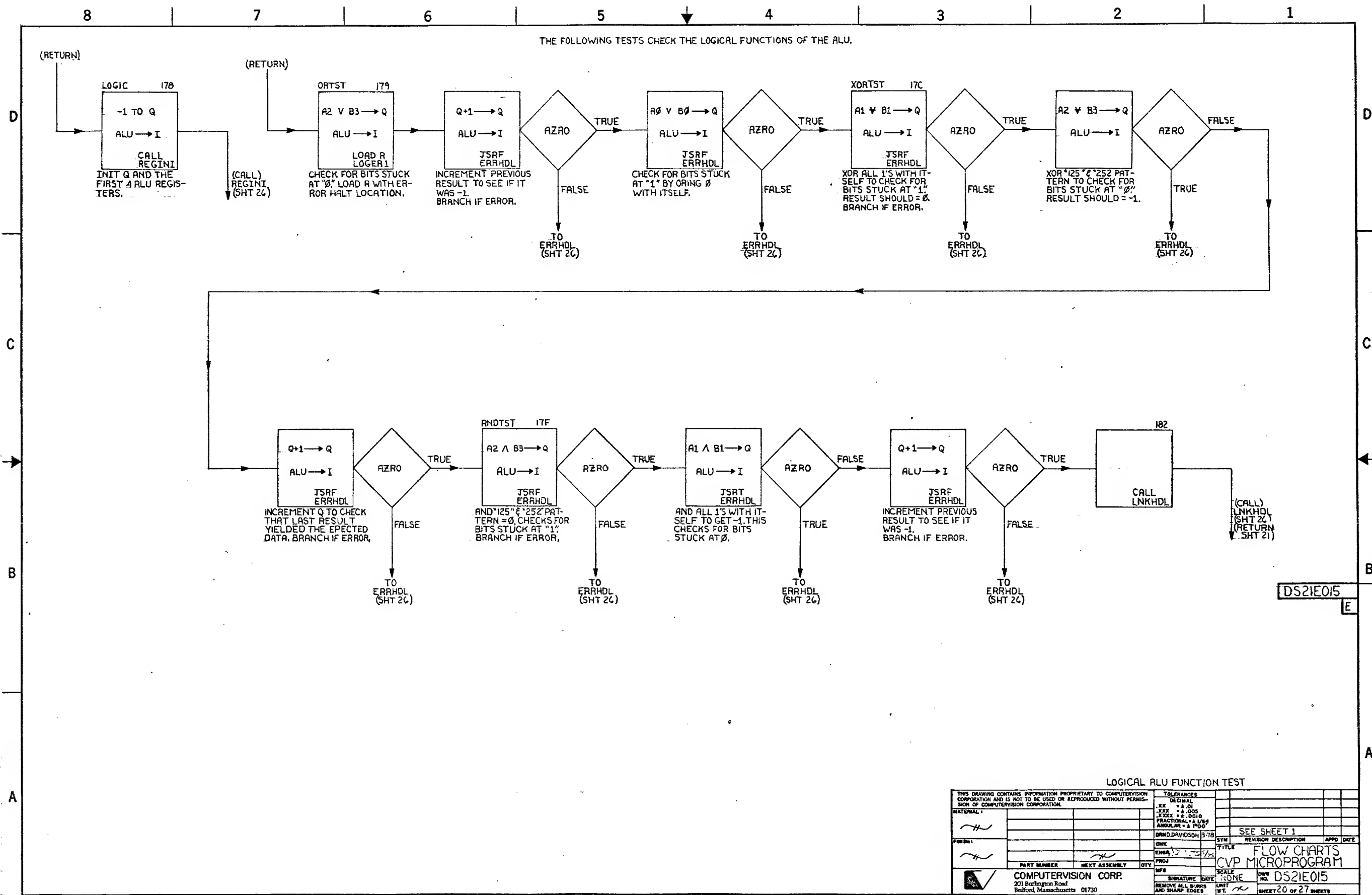






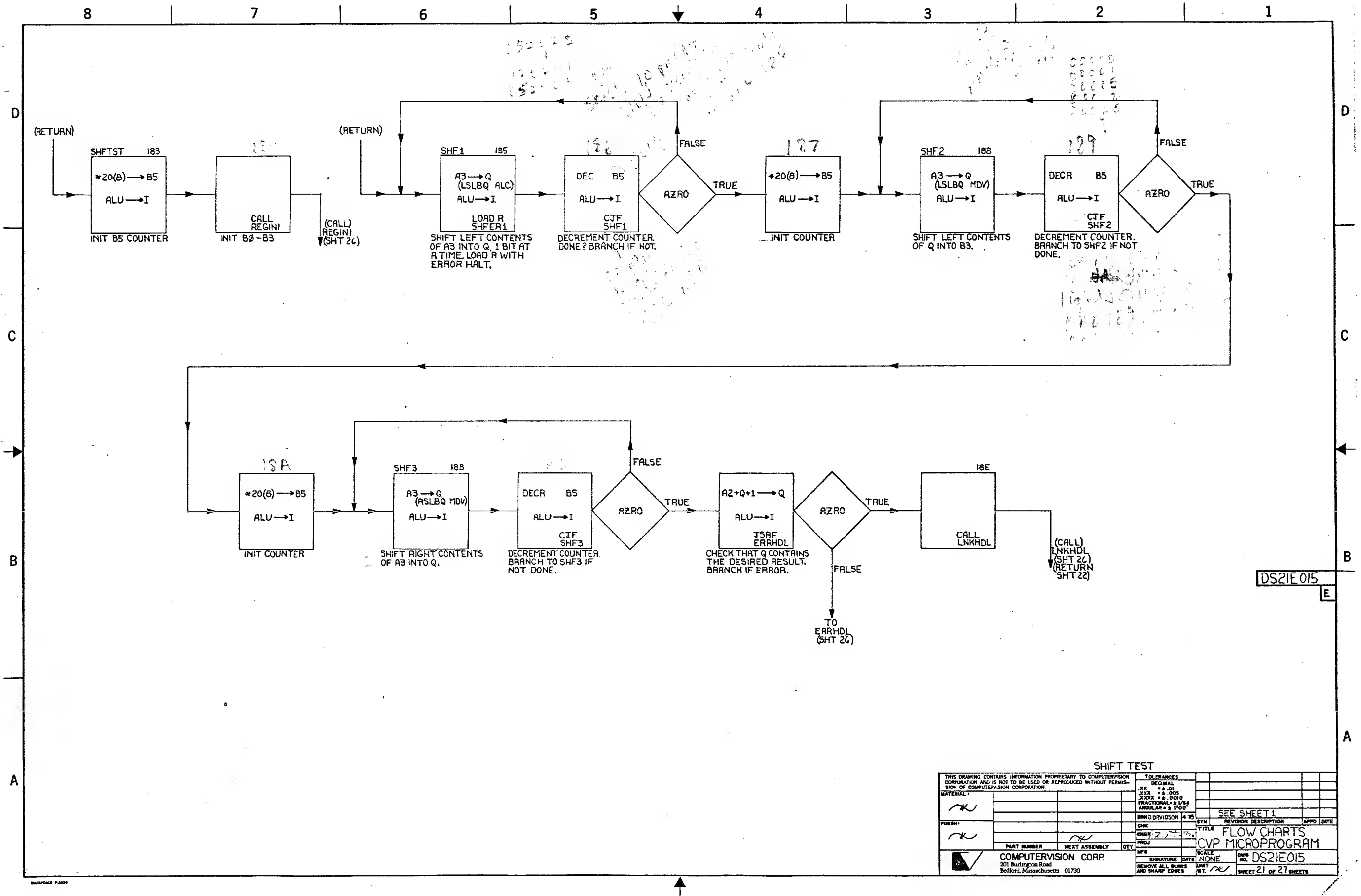


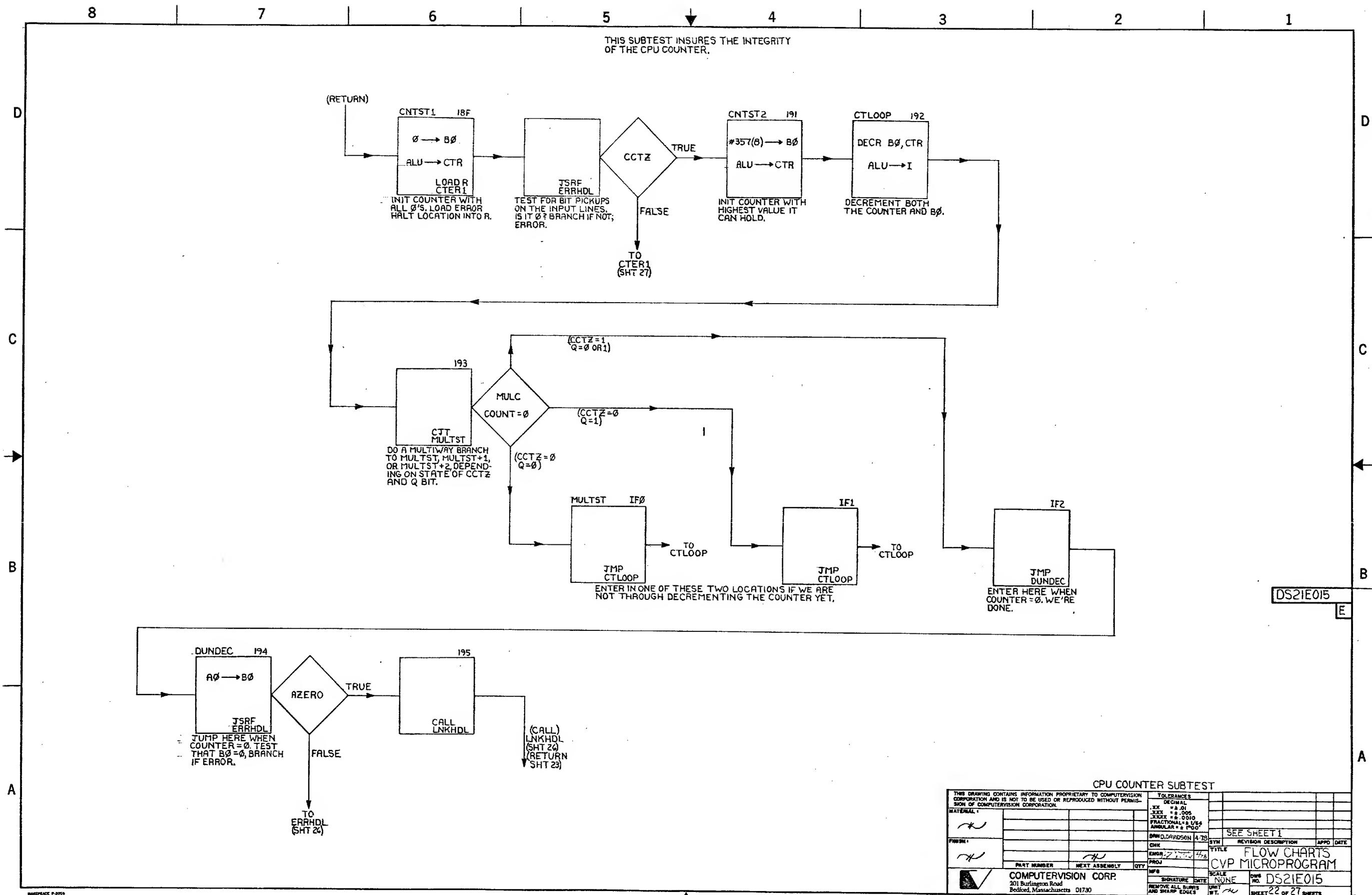




LOGICAL ALU FUNCTION TEST

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.				TOLERANCES DECIMAL XXX = ±.01 XXX = ±.005 XXX = ±.0010 FRACTIONAL = 1/64 ANGULAR = ±.0001		SYN REV DATE	
MATERIAL				DRWD. DAVIDSON 3-78		SEE SHEET 1	
PART NO.				CHK		TITLE	
PART NUMBER				ENGR. 1-1-78		FLOW CHARTS	
NEXT ASSEMBLY				PROJ		CVP MICROPROGRAM	
QTY				MFG		SCALE	
COMPUTERVISION CORP. 201 Burlington Road Bedford, Massachusetts 01730				SIGNATURE		NO. DS21E015	
REMOVE ALL BURRS AND SHARP EDGES				DATE		SHEET 20 OF 27 SHEETS	

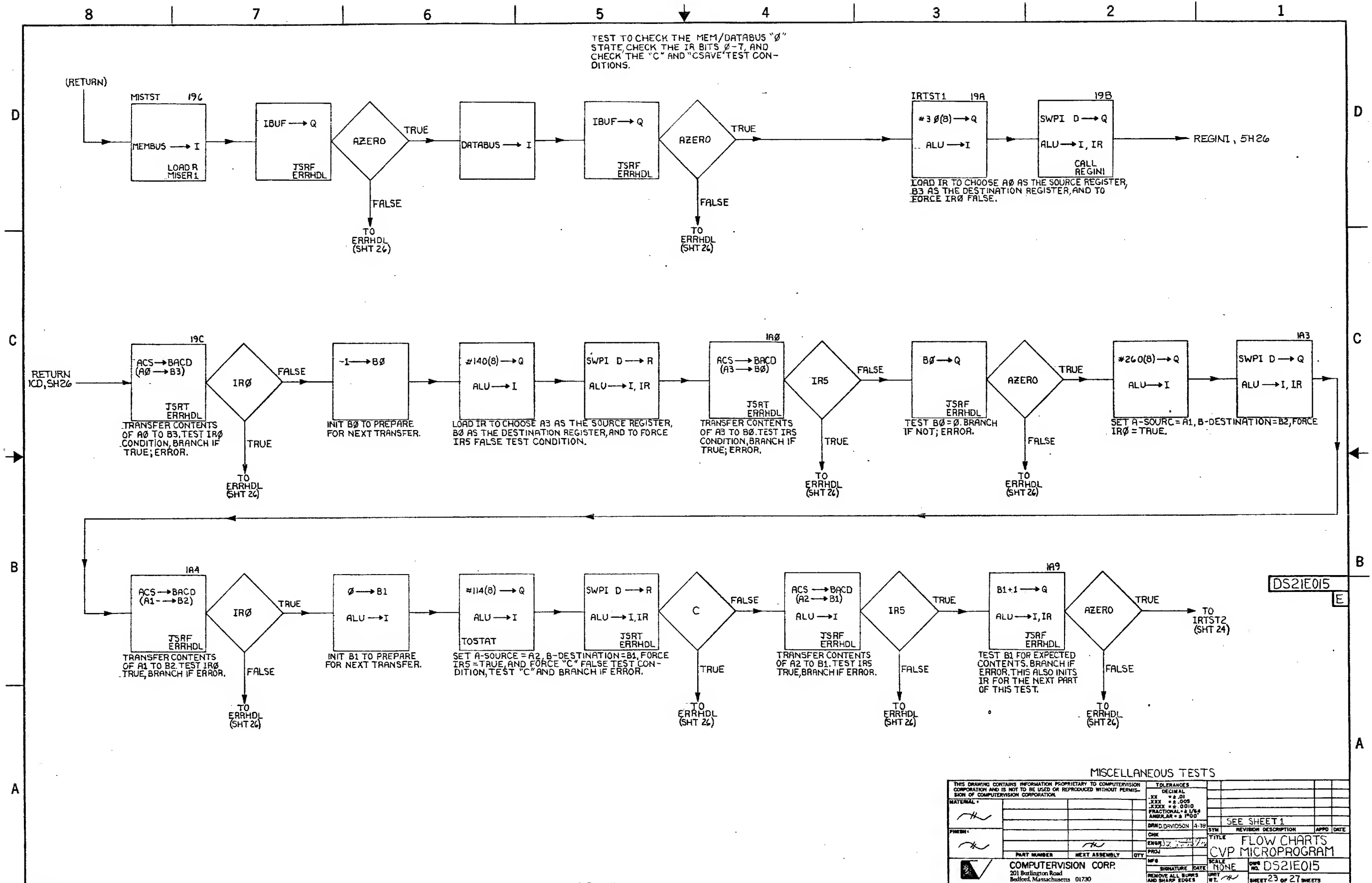


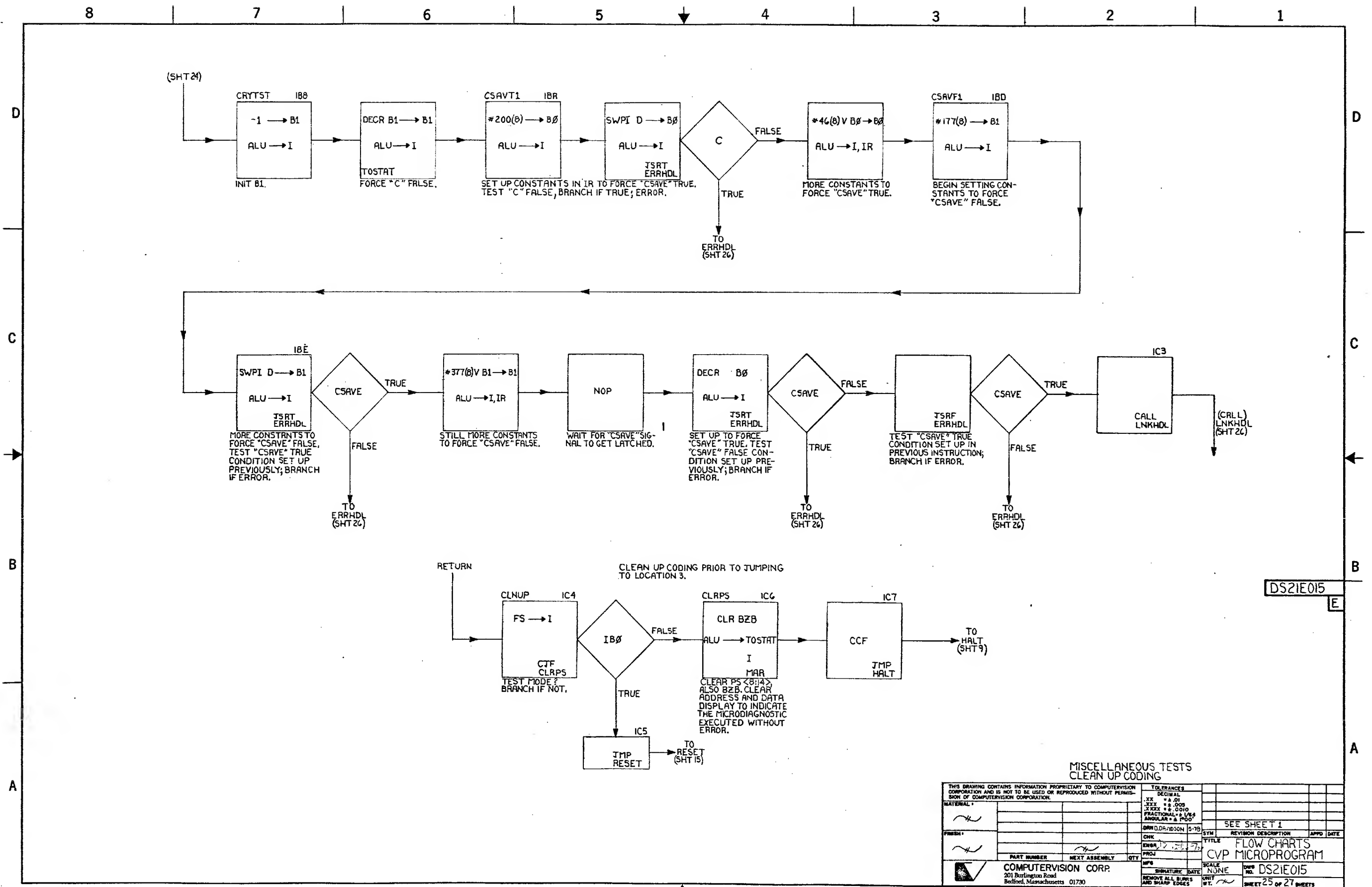


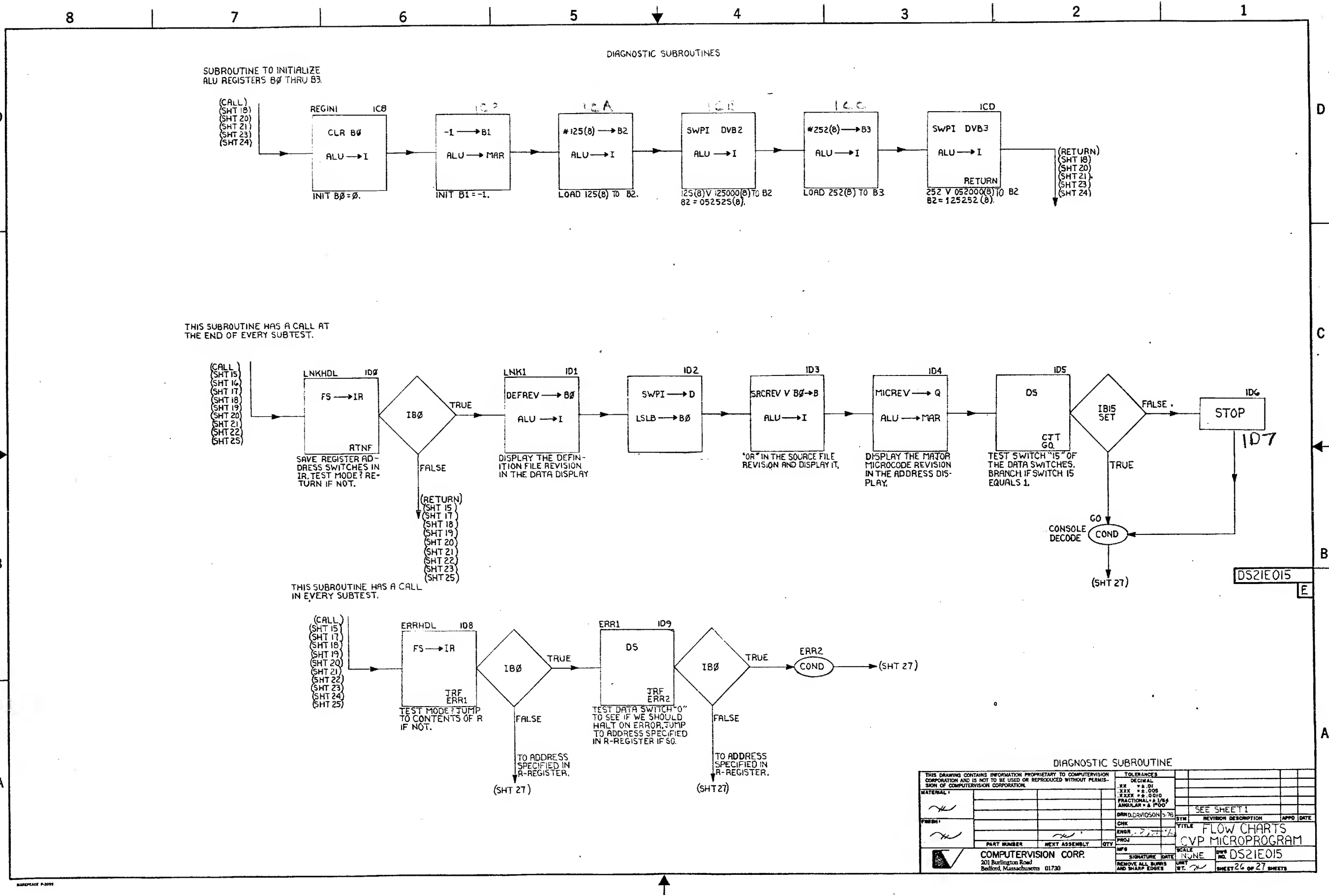
DS21E015

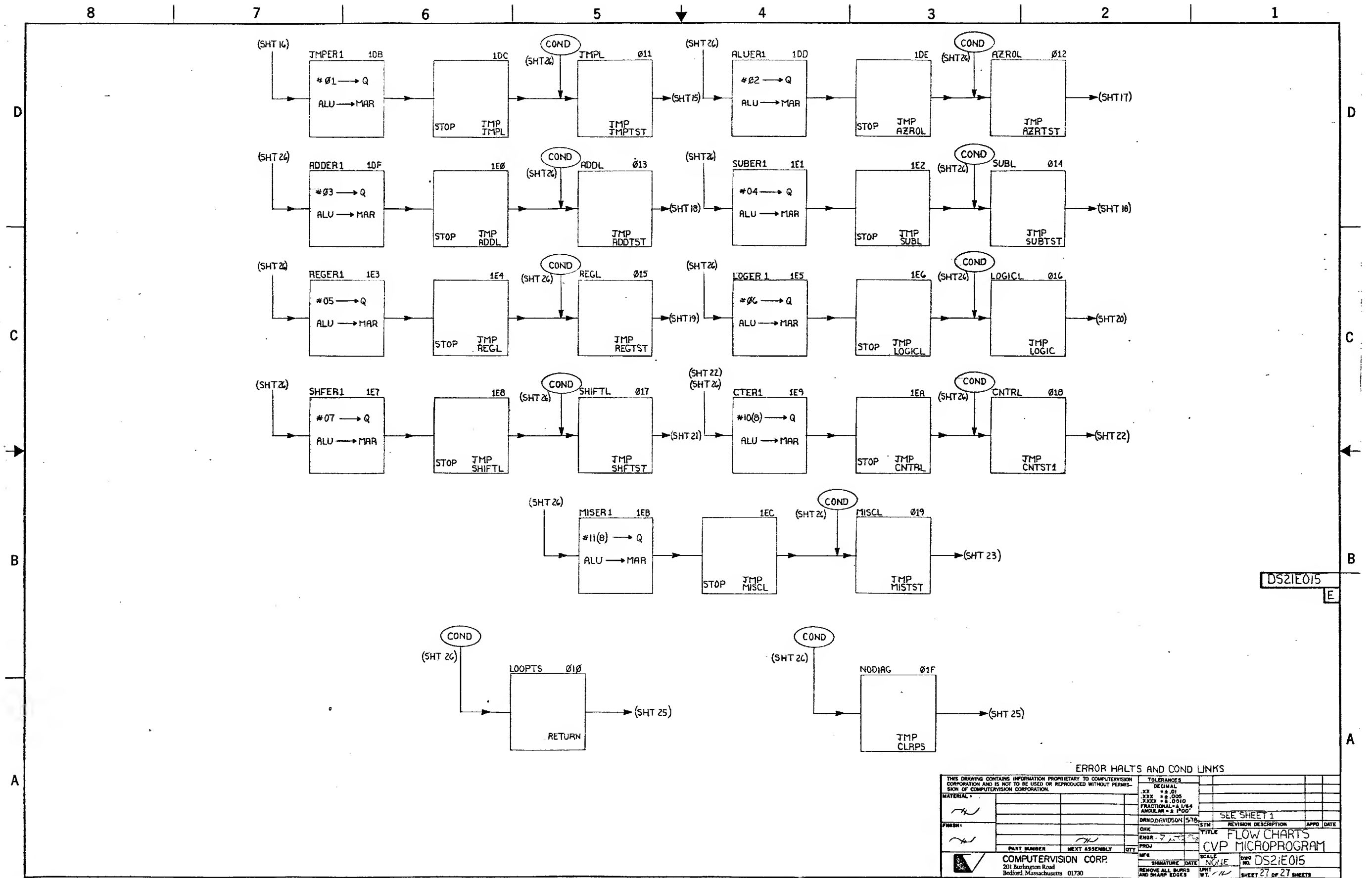
CPU COUNTER SUBTEST

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.		TOLERANCES DECIMAL XX = ±.01 XXX = ±.005 XXXX = ±.0010 FRACTIONAL = 1/64 ANGULAR = ± .001°			
MATERIAL:		DATE	4.75	SYN	SEE SHEET 1
FROM:		CHK		REV	
PROJ		ENG		DATE	
PART NUMBER		PROJ		TITLE	FLOW CHARTS CVP MICROPROGRAM
COMPUTERVISION CORP. 201 Burlington Road Bedford, Massachusetts 01730		SCALE	NONE	DWG NO.	DS21E015
		SIGNATURE		UNIT	
		REMOVE ALL BURRS AND SHARP EDGES		SHEET	22 OF 27 SHEETS









128/32K A/B-Port Memory Unit
DS21E252

	<u>Sheet No.</u>
Address Selection	1
Jumper Configuration	1
Memory Prioritizing	2
Refresh and Timing Logic	2
Data In Multiplexer	3
Data Out Latch	3
Parity Logic	3
Bus Control Logic	4
Bus Logic	5
Memory Address Logic	5
A-Port/B-Port Select Logic	6
Address Multiplexer Logic	6
Refresh Counter Logic	6
Row Address Strobe Clock	6
I/O Logic	7
Memory Row A	8
Memory Row B	9
Memory Row C	10
Memory Row D	11
Memory Row E	12
Memory Row F	13
Memory Row G	14
Memory Row H	15
B-Port Connectors	16

*1P2 on page 3-2
CSF 22 7000 001*

DA21E250-X CONFIGURATION TABLE

	SINGLE PORT	DUAL PORT, DISTRIBUTED MODE	DUAL PORT, GPU MODE	SINGLE PORT 32K
POPULATED WITH 4K RAMS (MK 4027-3)	USE CONFIGURATION BLOCKS A,A1,B	USE CONFIGURATION BLOCKS A,A1,C,D,E	USE CONFIGURATION BLOCKS A,C,D,E	
POPULATED WITH 16K RAMS (MK 4116-3)	DA21E250-02 USE CONFIGURATION BLOCKS B,F	DA21E250-01 USE CONFIGURATION BLOCKS D,E,F,G	DA21E250-01 USE CONFIGURATION BLOCKS E,F,H	DA21E250-03 USE CONFIGURATION BLOCKS A1,I

CONFIGURATION BLOCK A) 32K HARDWARE CONFIGURATION (USING 4K RAMS)

- 1) REMOVE R22
2) ADJUST POT R31 SUCH THAT TP HAS A 29 μ S REP RATE
3) INSERT JUMPERS: JP9-2, JP11-2, JP13-2
4) POPULATE MEMORY ARRAY WITH MK4027-3 MEMORY CHIPS

CONFIGURATION BLOCK A1) APORT 32K ADDRESSING CHART

*APORT FIELD	AMC0	AMC1	AMC2	AMC3	**CLOSED CONTACTS ON SWITCH PACK IV
0	H	H	H	H	8
1	H	H	H	L	7.8
2	H	H	L	H	8.B
3	H	H	L	L	8.7.8
4	H	L	H	H	6.8
5	H	L	H	L	5.7.8
6	H	L	L	H	5.8.8
7	H	L	L	L	5.8.7.8
8	L	H	H	H	4.8
9	L	H	H	L	4.7.8
10	L	H	L	H	4.8.8
11	L	H	L	L	4.B.7.8
12	L	L	H	H	4.5.8
13	L	L	H	L	4.5.7.8
14	L	L	L	H	4.5.B.B
15	L	L	L	L	4.5.B.7.8

- * EACH FIELD NO. REPRESENTS ONE 32K SEGMENT OF MEMORY
** ALL OTHER CONTACTS ON SWITCH PACK IV OPEN

CONFIGURATION BLOCK B) SINGLEPORT CONFIGURATION

- 1) DEPOPULATE PC BOARD AS PER BM21E250-02
2) ADD JUMPERS JP3, JP6, JP7

CONFIGURATION BLOCK C) BPORT 32K MEMORY ROW SELECT

- 1) INSERT JUMPERS: JP10-2, JP12-2, JP14-2

CONFIGURATION BLOCK D) BPORT 32K ADDRESSING AND I/O DEVICE CODE CHART

*BPORT FIELD OR I/O DEVICE CODE	BMC0 OR BDS0	BMC1 OR BDS1	BMC2 OR BDS2	BMC3 OR BDS3	**CLOSED CONTACTS ON SWITCH PACK 12S
0	H	H	H	H	8
1	H	H	H	L	4.8
2	H	H	L	H	3.8
3	H	H	L	L	3.4.8
4	H	L	H	H	2.8
5	H	L	H	L	2.4.8
6	H	L	L	H	2.3.B
7	H	L	L	L	2.3.4.8
8	L	H	H	H	1.8
9	L	H	H	L	1.4.B
10	L	H	L	H	1.3.B
11	L	H	L	L	1.3.4.B
12	L	L	H	H	1.2.8
13	L	L	H	L	1.2.4.8
14	L	L	L	H	1.2.3.8
15	L	L	L	L	1.2.3.4.8

- * EACH FIELD NO. REPRESENTS ONE 32K SEGMENT OF MEMORY
** ALL OTHER CONTACTS ON SWITCH PACK 12S AND 9C OPEN

CONFIGURATION BLOCK E) LAST BOARD IN DAISY CHAIN

THE LAST DUAL PORT MEMORY BOARD IN A DAISY CHAIN MUST TERMINATE BPORT BUS SIGNALS. THE LAST DUAL PORT MEMORY IN A DAISY CHAIN ONLY MUST HAVE THE FOLLOWING RESISTORS: RP6,RP7,RP8, RP12, RES PACK 12F

CONFIGURATION BLOCK F) 128K HARDWARE CONFIGURATION/APORT 128K ADDRESSING M

- 1) R20 AND R22 INSERTED
2) INSERT JIMPER JP4
3) ADJUST POT R31 SUCH THAT TP HAS A 14.5 μ S REP RATE
4) INSERT JUMPERS JP9, JP11, JP13
5) POPULATE MEMORY ARRAY WITH MK411B-3 MEMORY CHIPS
6) APORT 128K ADDRESSING CHART

*APORT FIELD NO.	AMC0	AMC1	AMC2	AMC3	AMC3	**CLOSED CONTACTS ON SWITCH PACK IV
0.1.2.3	H	H	H	H	H	
4.5.6.7	H	H	H	H	L	6
8.9.10.11	H	H	H	L	H	4
12.13.14.15	H	H	H	L	L	4.5
16.17.18.19	H	H	L	H	H	3
20.21.22.23	H	H	L	H	L	3.6
24.25.26.27	H	H	L	L	H	3.4
28.29.30.31	H	H	L	L	L	3.4.6
32.33.34.35	H	L	H	H	H	2
36.37.38.39	H	L	H	H	L	2.6
40.41.42.43	H	L	H	L	H	2.4
44.45.46.47	H	L	H	L	L	2.4.6
48.49.50.51	H	L	L	H	H	2.3
52.53.54.55	H	L	L	H	L	2.3.6
56.57.58.59	H	L	L	L	H	2.3.4
60.61.62.63	H	L	L	L	L	2.3.4.6
64.65.66.67	L	H	H	H	H	1
68.69.70.71	L	H	H	H	L	1.6
72.73.74.75	L	H	H	L	H	1.4
76.77.78.79	L	H	H	L	L	1.4.6
80.81.82.83	L	H	L	H	H	1.3
84.85.86.87	L	H	L	H	L	1.3.6
88.89.90.91	L	H	L	L	H	1.3.4
92.93.94.95	L	H	L	L	L	1.3.4.6
96.97.98.99	L	L	H	H	H	1.2
100.101.102.103	L	L	H	H	L	1.2.6
104.105.106.107	L	L	H	L	H	1.2.4
108.109.110.111	L	L	H	L	L	1.2.4.6
112.113.114.115	L	L	L	H	H	1.2.3
116.117.118.119	L	L	L	H	L	1.2.3.6
120.121.122.123	L	L	L	L	H	1.2.3.4
124.125.126.127	L	L	L	L	L	1.2.3.4.6

- * EACH FIELD NO. REPRESENTS ONE 32K SEGMENT OF MEMORY
(TO EXPAND BEYOND 15 FIELDS, IC 2X AND 2V, SHT.7, MUST BE ADDED)
** ALL OTHER SWITCH CONTACTS ON SWITCH IV ARE OPEN

CONFIGURATION BLOCK G) 128K APORT/32K BPORT COMMON MEMORY

WITH JUMPERS JP10, JP12, JP14, INSERTED

BMC2	BMC3	COMMON SEGMENT OF APORT 128K MEMORY
H	H	1ST 32K
H	L	2ND 32K
L	H	3RD 32K
L	L	4TH 32K

- 2) TO FORCE COMMON APORT/BPORT MEMORY
INDEPENDENT OF BMC2 AND BMC3

BMC2	BMC3	COMMON SEGMENT OF APORT 128K MEMORY	JUMPERS INSERTED
X	X	1ST 32K	JP10, JP15, JP18
X	X	2ND 32K	JP10, JP18
X	X	3RD 32K	JP10, JP15
X	X	4TH 32K	JP10

WHERE X = DONT CARE

CONFIGURATION BLOCK H) BPORT 128K ADDRESSING CONFIGURATION

- 1) INSERT JUMPERS JP10, JP12, JP14
2) BPORT 128K ADDRESSING CHART

BPORT FIELD NO.	BMAD0	BMAD1	BMAD2	BMC0	BMC1	**CLOSED CONTACTS ON SWITCH PACKS
						9C 12S
0.1.2.3	H	H	H	H	H	8
4.5.6.7	H	H	H	H	L	2.8
8.9.10.11	H	H	H	L	H	1.8
12.13.14.15	H	H	H	L	L	1.2.8
16.17.18.19	H	H	L	H	H	8
20.21.22.23	H	H	L	H	L	7 2.8
24.25.26.27	H	H	L	L	H	7 1.8
28.29.30.31	H	H	L	L	L	7 1.2.8
32.33.34.35	H	L	H	H	H	8 8
36.37.38.39	H	L	H	H	L	8 2.8
40.41.42.43	H	L	H	L	H	8 1.8
44.45.46.47	H	L	H	L	L	8 1.2.8
48.49.50.51	H	L	L	H	H	8.7 8
52.53.54.55	H	L	L	H	L	8.7 2.8
56.57.58.59	H	L	L	L	H	8.7 1.8
60.61.62.63	H	L	L	L	L	8.7 1.2.8
64.65.66.67	L	H	H	H	H	5 8
68.69.70.71	L	H	H	H	L	5 2.8
72.73.74.75	L	H	H	L	H	5 1.8
76.77.78.79	L	H	H	L	L	5 1.2.8
80.81.82.83	L	H	L	H	H	5.7 8
84.85.86.87	L	H	L	H	L	5.7 2.8
88.89.90.91	L	H	L	L	H	5.7 1.8
92.93.94.95	L	H	L	L	L	5.7 1.2.8
96.97.98.99	L	L	H	H	H	5.8 8
100.101.102.103	L	L	H	H	L	5.8 2.8
104.105.106.107	L	L	H	L	H	5.8 1.8
108.109.110.111	L	L	H	L	L	5.8 1.2.8
112.113.114.115	L	L	L	H	H	5.B.7 8
116.117.118.119	L	L	L	H	L	5.8.7 2.8
120.121.122.123	L	L	L	L	H	5.8.7 1.8
124.125.126.127	L	L	L	L	L	5.8.7 1.2.8

- EACH FIELD NO. REPRESENTS ONE 32K SEGMENT OF MEMORY
ALL OTHER CONTACTS ON SWITCH PACK 12S AND 9C OPEN
(9C-2 MAY BE CLOSED TO DISABLE APORT)

CONFIGURATION BLOCK I) 32K SINGLE PORT CONFIGURATION (USING 18K RAMS)

- 1) DEPOPULATE BOARDS AS PER ASSEMBLY DA21E250-03

MISCELLANEOUS JUMPERS

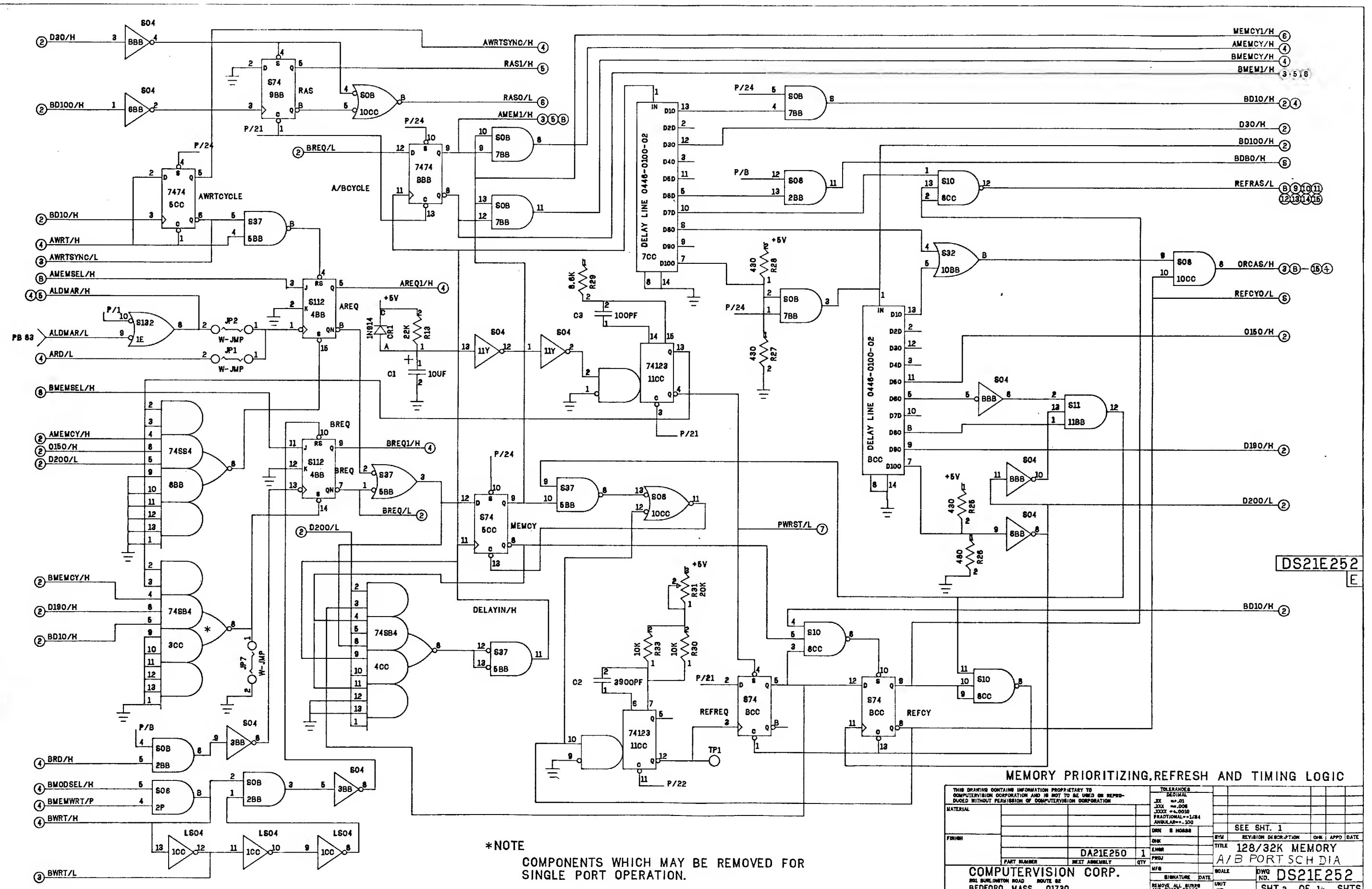
- 1) FOR LDMA STARTING APORT MEMORY CYCLE INSERT JP-2
2) FOR MEMREAD STARTING APORT MEMORY CYCLE INSERT JP-1
3) FOR GPU MODE REQUIRING DISABLED APORT, CLOSE SWITCH 9C-2
4) APORT MUC/NON MUC OPERATION

JUMPER PLUG 4D	
MUC OPERATION	1-18 2-15 3-14 4-13
NON MUC OPERATION	5-12 6-11 7-10 8-9

- 5) APORT I/O DEVICE CODE

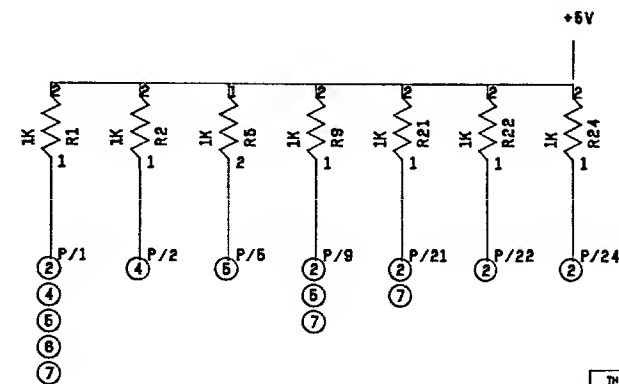
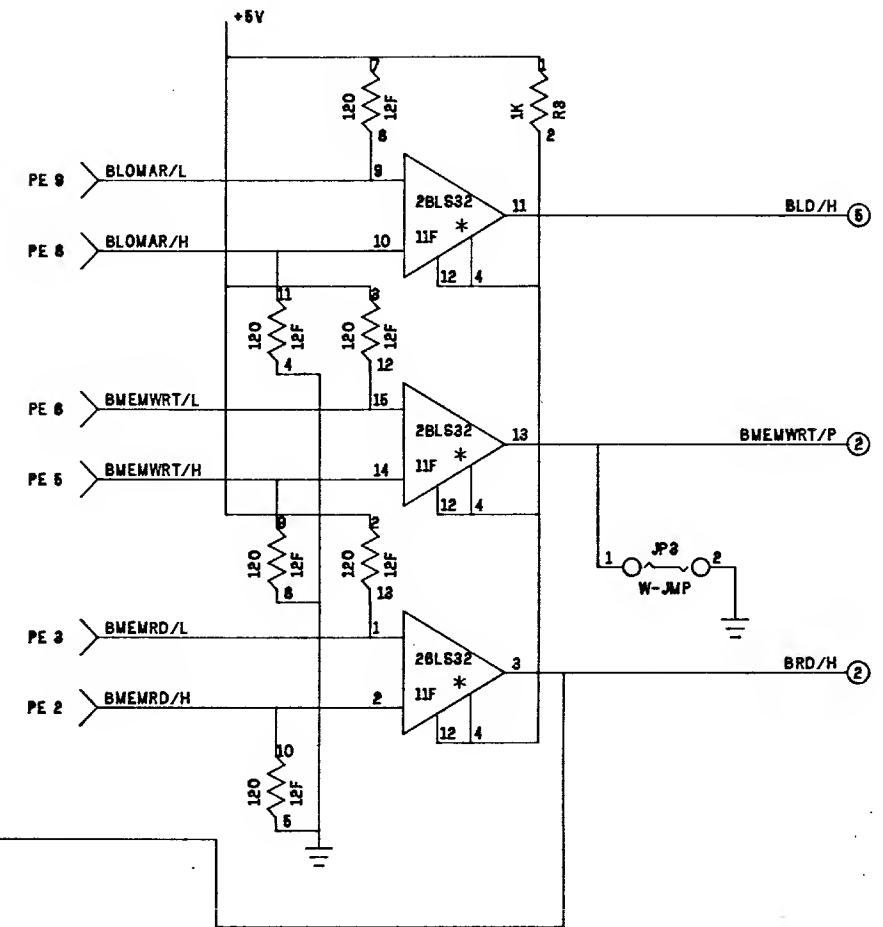
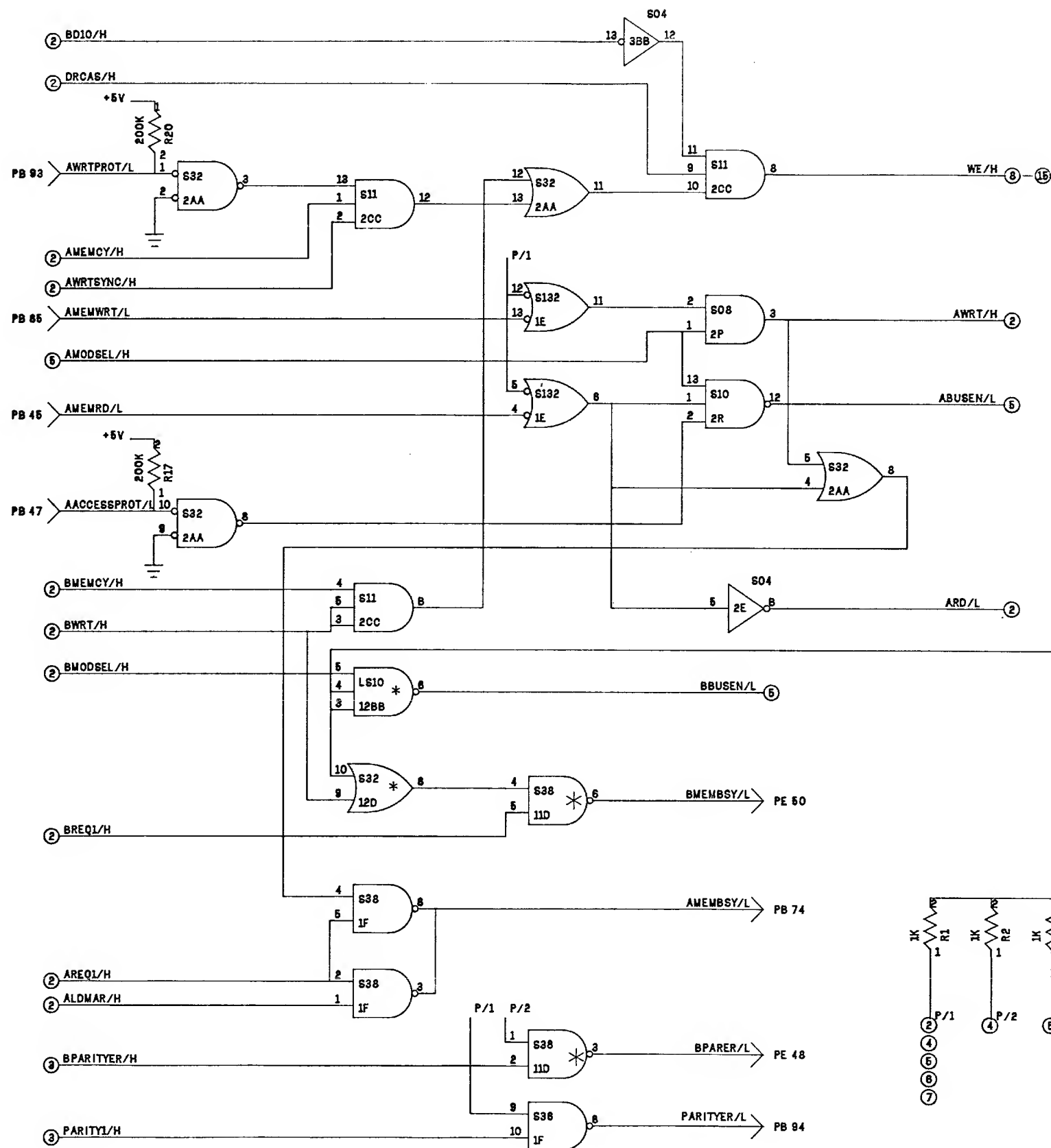
- 1) STANDARD 24₈, INSERT JP8 FOR 25₈

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MATERIAL		DNR 8 HOBBS		D ECO 33.8	
FINISH		ENGR 11/11/79		REV DESCRIPTION DATE	
PART NUMBER		DA21E250		TITLE 128/32K MEMORY	
NEXT ASSEMBLY		QTY 1		V/B PORT SCH. 3 AGRAM	
COMPUTERVISION CORP.				SCALE	
801 BURLINGTON ROAD ROUTE 88 BEDFORD, MASS. 01730				DWD NO. DS21E252	
REMOVE ALL BURRS AND SHARP EDGES				UNIT SHT 1 OF 16 SHTS	



MEMORY PRIORITIZING, REFRESH AND TIMING LOGIC

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPROD- UCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION				TOLERANCES UNLESS OTHERWISE SPECIFIED XX .XX XXX .XXX XXXX .XXXX FRACTIONAL = 1/64 ANGULAR = .100			
MATERIAL				DRN	5	NOV88	
FINISH				ENMR			
				PROJ			
				MFB			
				SIGNATURE	DATE		
				REMOVE ALL BURRS AND SHARP EDGES	UNIT		
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					DATE		
					REV		
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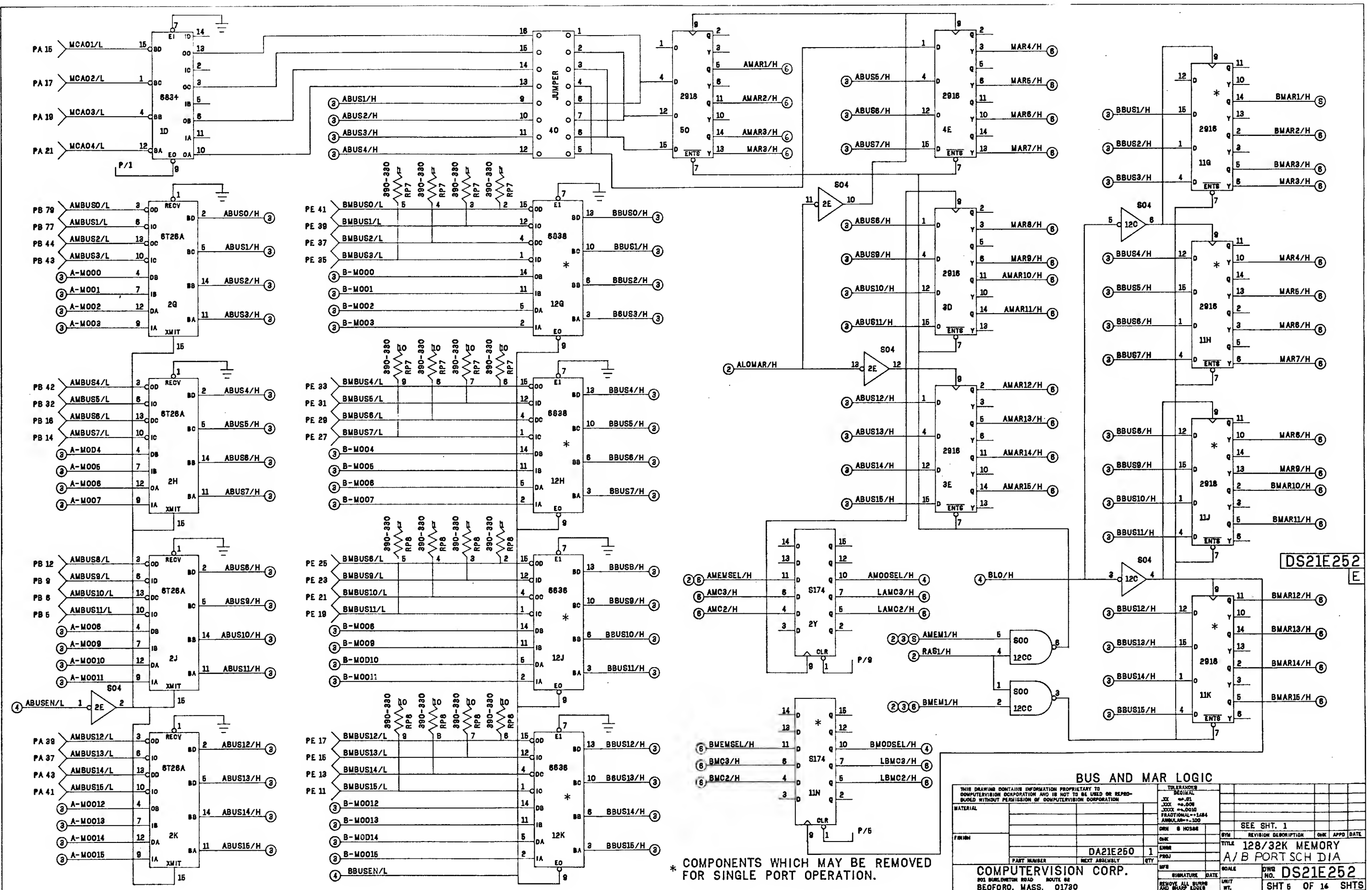


*NOTE:
COMPONENTS WHICH MAY BE REMOVED
FOR SINGLE PORT OPERATION.

DS21E252
E

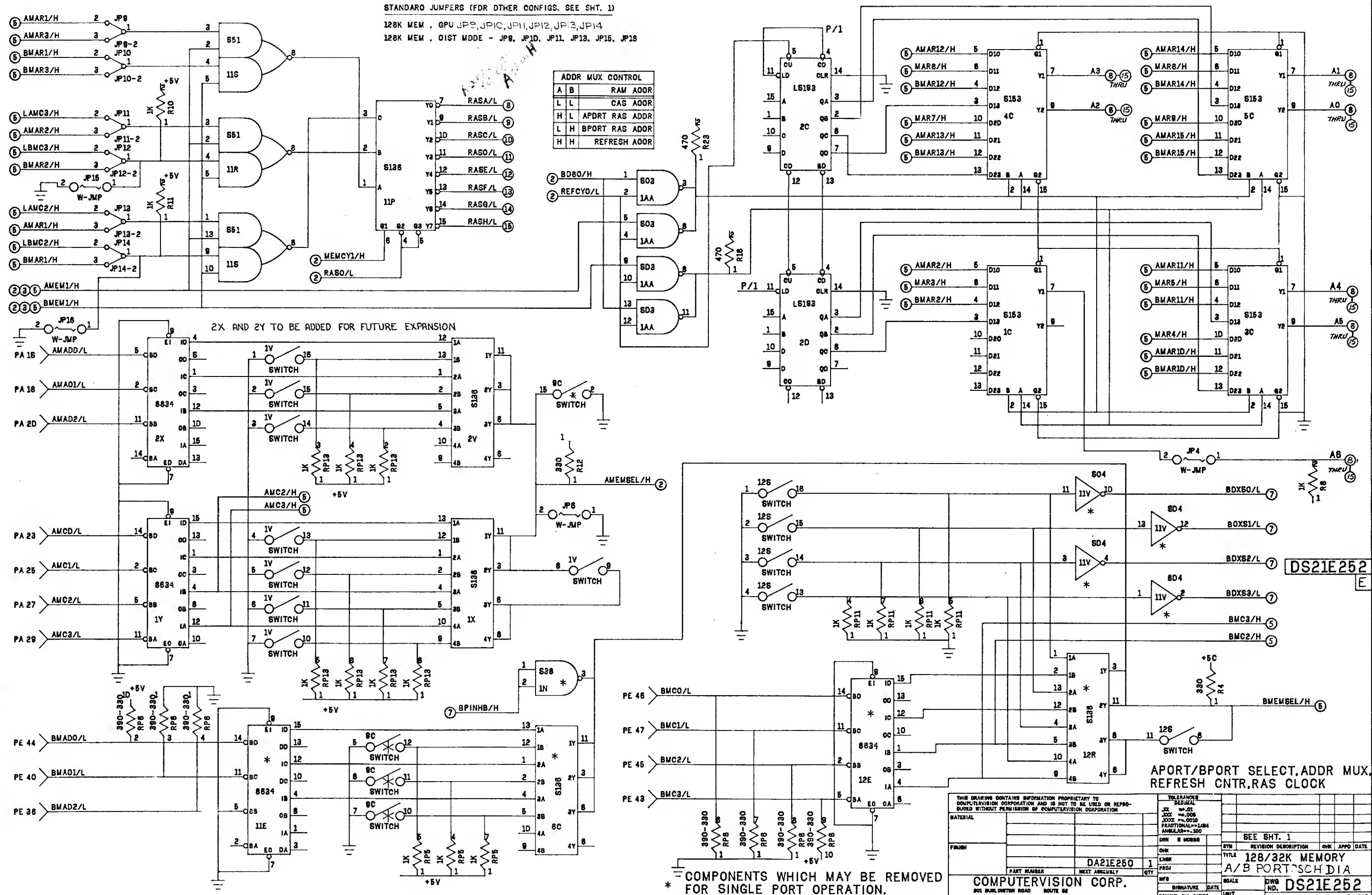
BUS CONTROL LOGIC

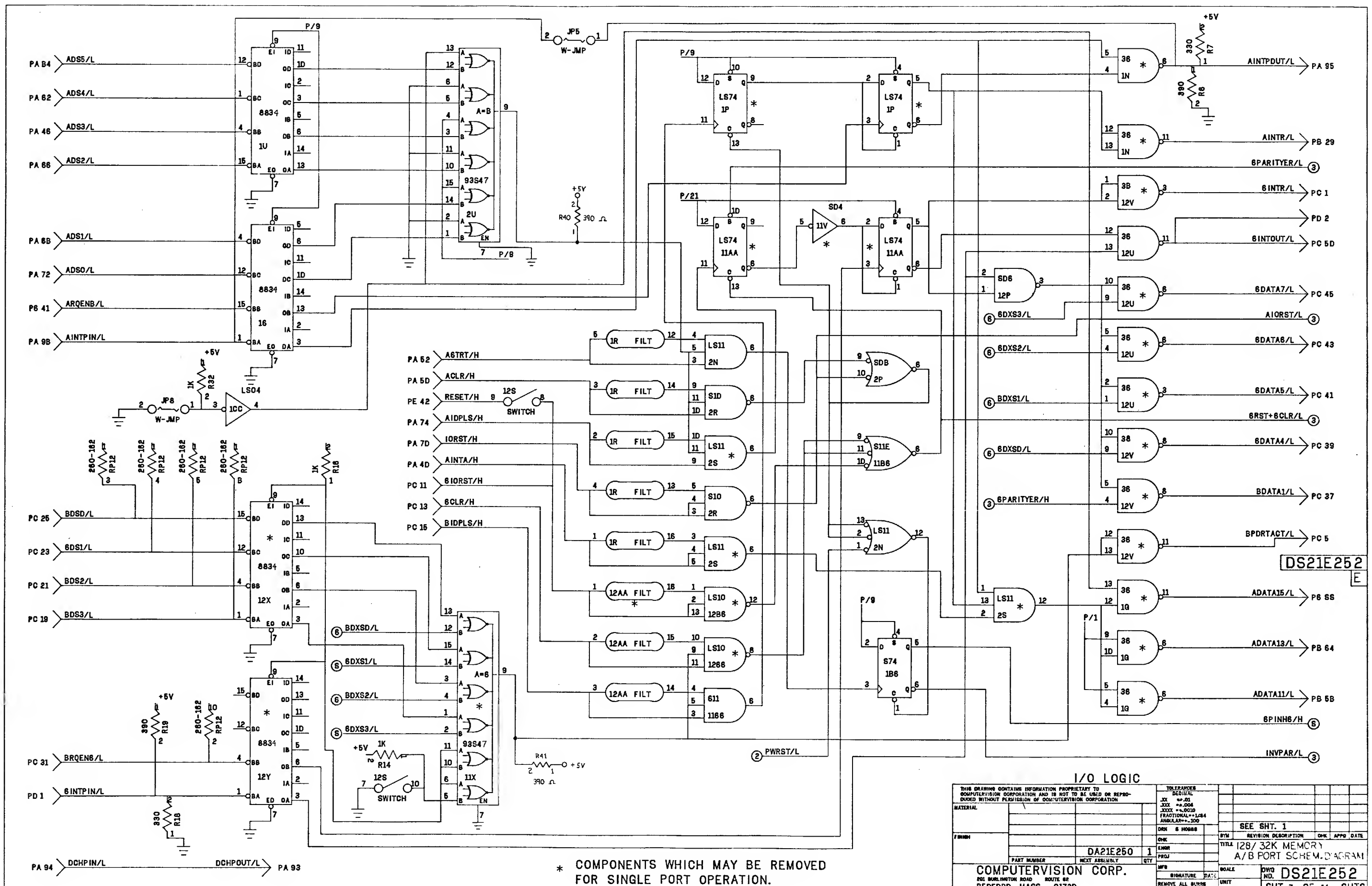
THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION				TOLERANCES DECIMAL XX .XX XXX .XXX XXXX .XXXX FRACTIONAL 1/64 ANGULAR .100			
MATERIAL				DRN	B HOBBS	SEE SHT. 1	
FINISH				CHK		REV	REVISION DESCRIPTION
				ENGR		DATE	128/32K MEMORY
				PROJ		UNIT	A/B PORT SCH DIA
PART NUMBER	DA21E250	1	QTY	DATE		NO.	DS21E252
COMPUTERVISION CORP. 201 BURLINGTON ROAD ROUTE 62 BEDFORD, MASS. 01730				SIGNATURE	DATE	UNIT	SHT 4 OF 16 SHTS



* COMPONENTS WHICH MAY BE REMOVED FOR SINGLE PORT OPERATION.

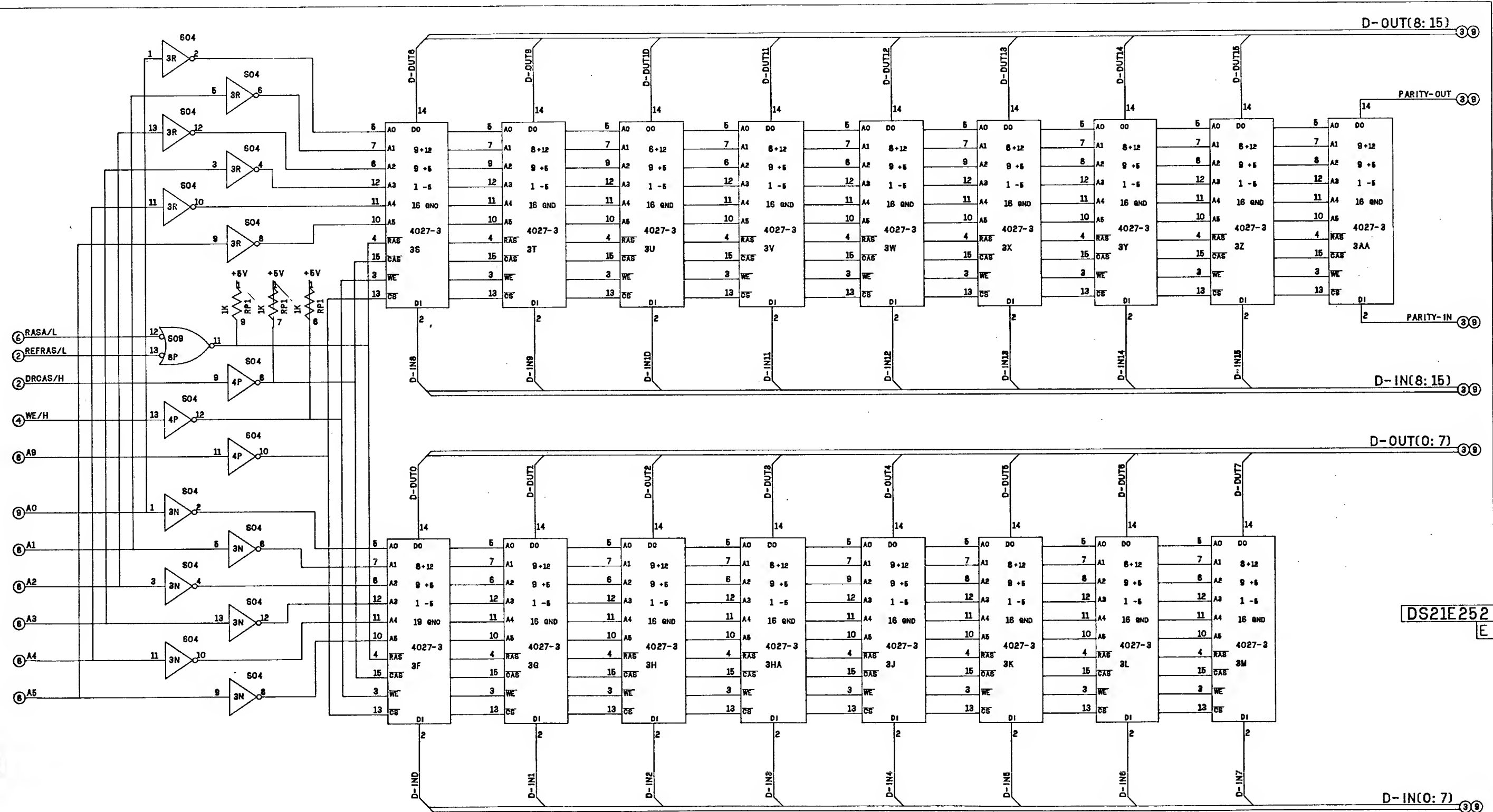
BUS AND MAR LOGIC		TOLERANCES	
THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTATION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTATION CORPORATION		UNLESS OTHERWISE SPECIFIED	
MATERIAL		XX .01	
FINISH		XX .005	
PART NUMBER		DA21E250	
NEXT ASSEMBLY		1	
COMPUTATION CORP.		DA21E250	
100 BURLINGTON ROAD ROUTE 66		DA21E250	
BEDFORD, MASS. 01730		DA21E250	
SEE SHT. 1		SEE SHT. 1	
TITLE		128/32K MEMORY	
A/B PORT SCH DIA		A/B PORT SCH DIA	
SIGNATURE		DATE	
REMOVE ALL BURRS AND SHARP EDGES		UNIT	
SHT 5 OF 16 SHTS		SHT 5 OF 16 SHTS	





* COMPONENTS WHICH MAY BE REMOVED
FOR SINGLE PORT OPERATION.

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION						TOLERANCES DECIMAL ±.01 ±.008 ±.0010 FRACTIONAL ± 1/64 ANGULAR ± .005					
MATERIAL						DWG NO.	DS21E252	SHT	7	OF	16
FINISH						TITLE	128/ 32K MEMORY A/B PORT SCHEM. DIAGRAM				
PART NUMBER	DA21E250	1	QTY								
NEXT ASSEMBLY											
COMPUTERVISION CORP. PO BOX BURLINGTON ROAD ROUTE 62 BEDFORD, MASS. 01730						SIGNATURE DATE					
						UNIT WT.					

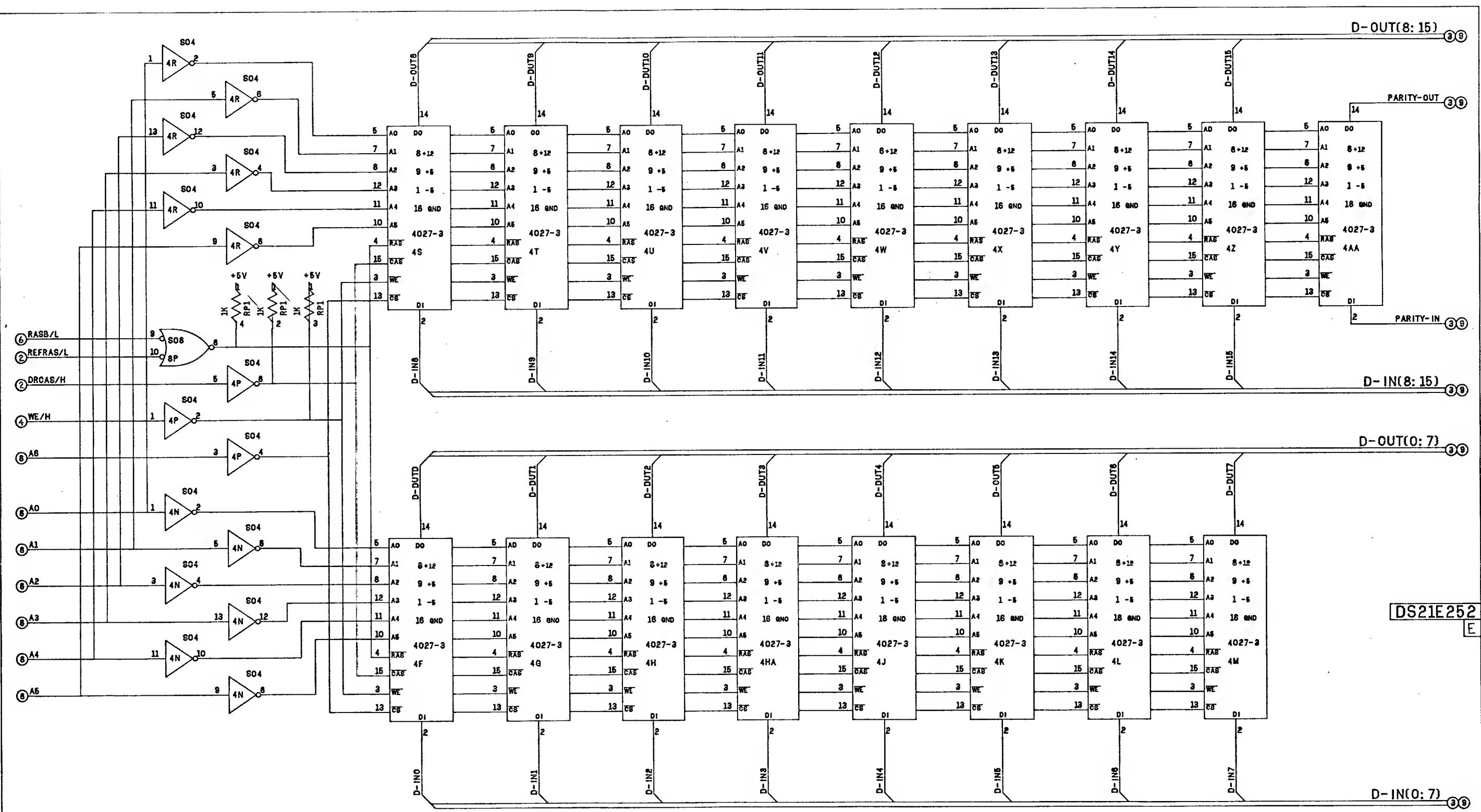


MEMORY CHIPS 3S THRU 3AA
AND 3F THRU 3M MAY BE
EITHER ALL 4027-3 OR
4116-3 PARTS

DS21E252
E

MEMORY ROW A

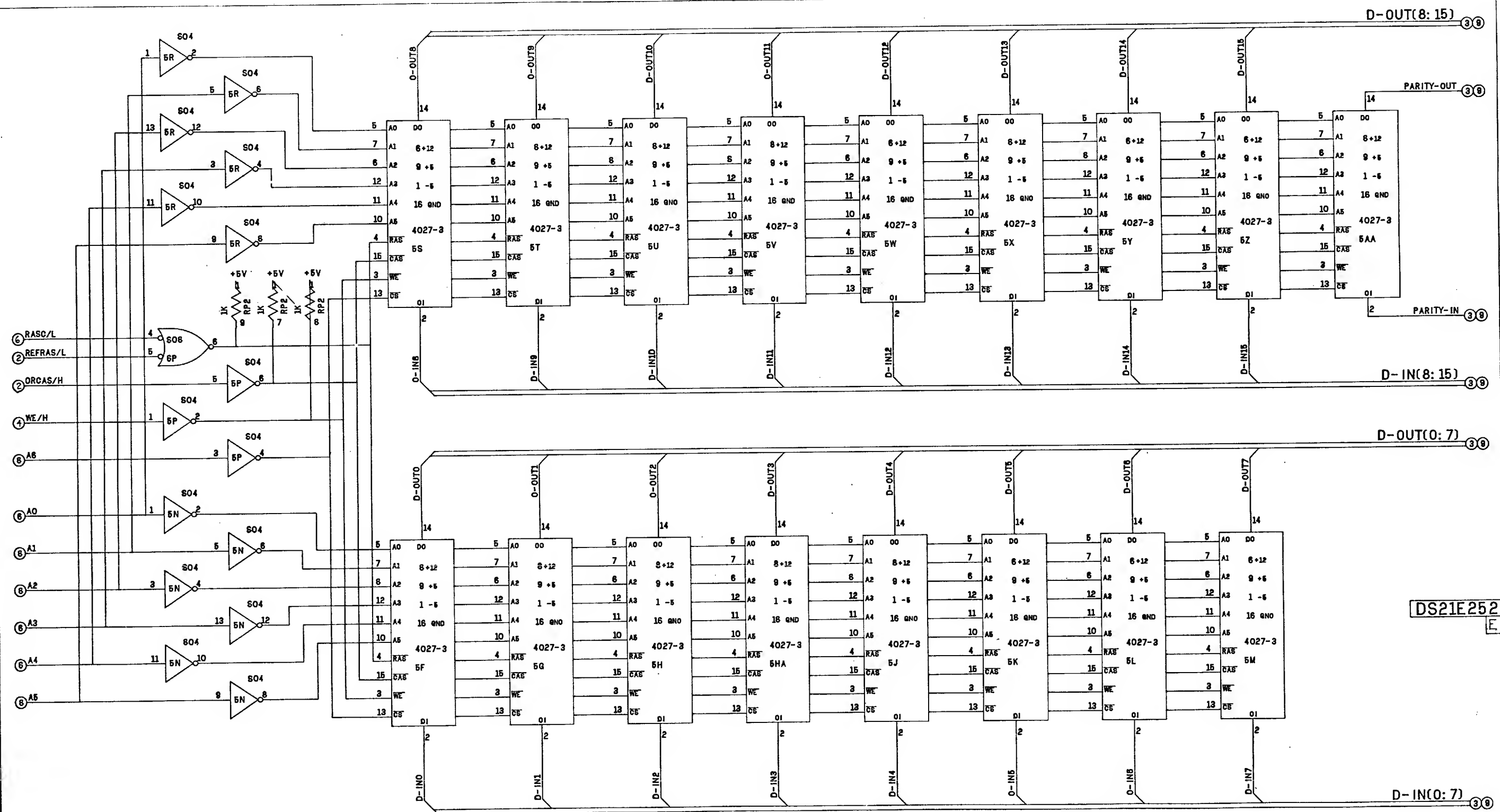
THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRO- DUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION		TOLERANCES DECIMAL XX .XX XXX .XXX XXXX .XXXX FRACTIONAL ANGULAR			
MATERIAL		DWG NO.	1	REV	1
FINISH		DATE		BY	
PART NUMBER	DA21E250	QTY	1	REVISION DESCRIPTION	SEE SHT. 1
COMPUTERVISION CORP. 201 BURLINGTON ROAD BEDFORD, MASS. 01730		SIGNATURE		DATE	
REMOVE ALL BURRS AND SHARP EDGES		UNIT WT.		DWG NO. DS21E252	
				SHT 9 OF 16 SHTS	



MEMORY CHIPS 4S THRU 4AA
AND 4F THRU 4M MAY BE
EITHER ALL 4027-3 OR
4116-3 PARTS

DS21E252
E

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRO- DUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION				TOLERANCES UNLESS SPECIFIED ALL DIMENSIONS FRACTIONAL - 1/64 ANGULAR - 1/16				REVISION DESCRIPTION			
MATERIAL				SEE SHT. 1				DATE			
FINISH				ONE				DATE			
PART NUMBER				DA21E250				DATE			
NEXT ASSEMBLY				QTY				DATE			
COMPUTERVISION CORP.				SIGNATURE				DATE			
303 BURLINGTON ROAD ROUTE 88 BEDFORD, MASS. 01730				UNIT				DATE			
				WT.				DATE			
				SHT 9 OF 16 SHTS							

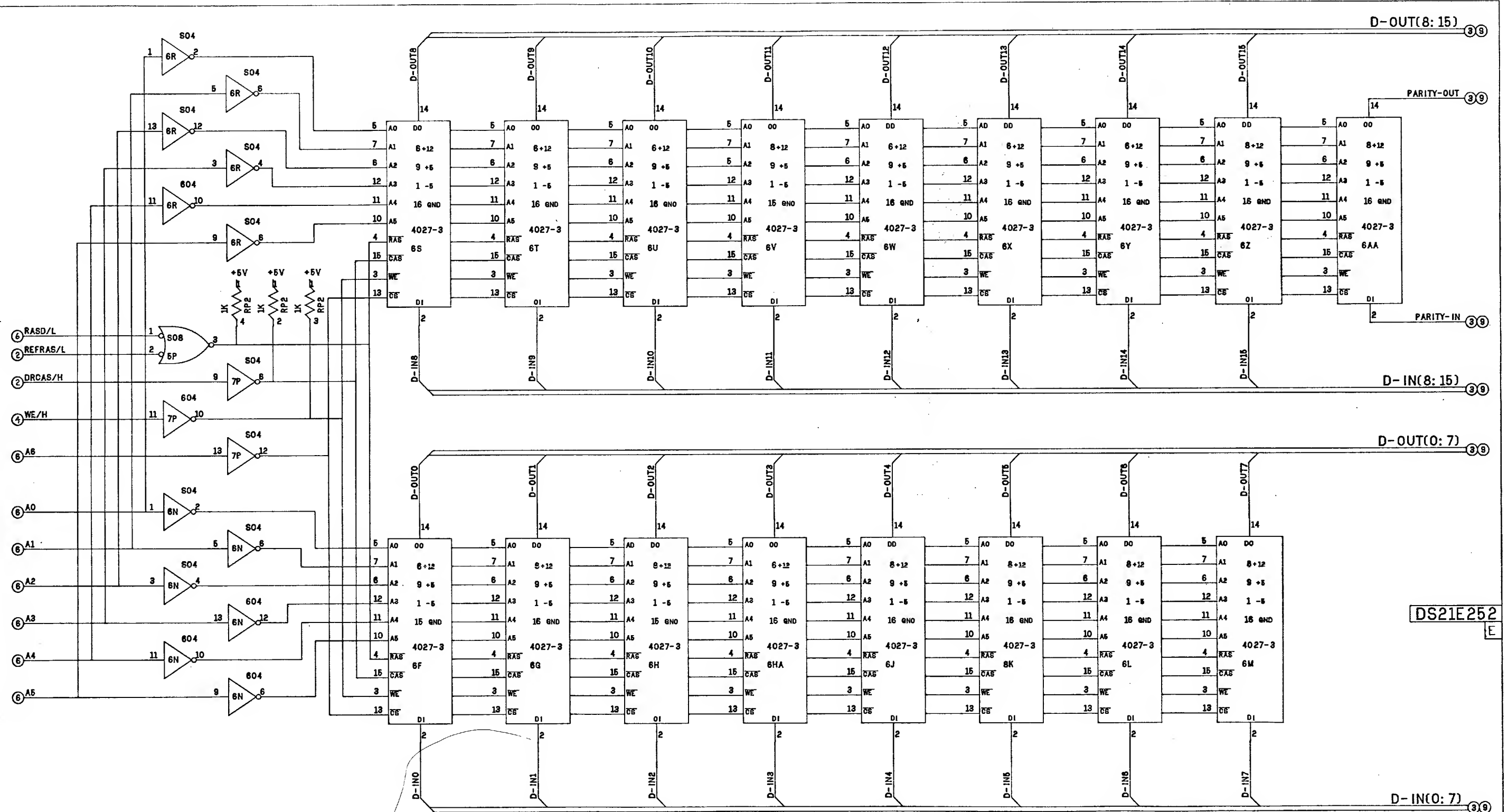


MEMORY CHIPS 5S THRU 5AA
AND 5F THRU 5M MAY BE
EITHER ALL 4027-3 OR
4116-3 PARTS

DS21E252
E

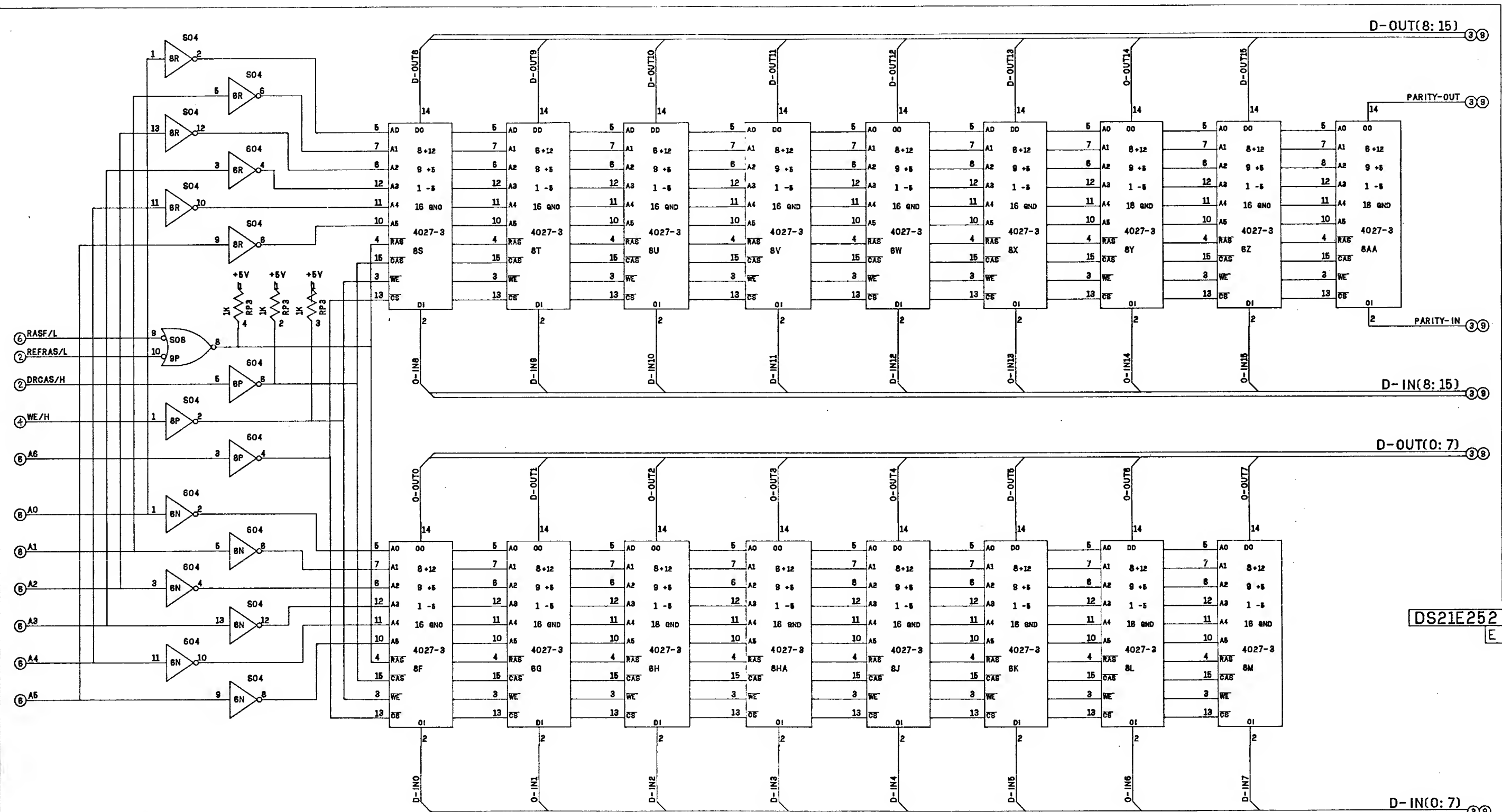
MEMORY ROW C

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRO- DUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION		TOLERANCES DECIMAL XX .XX XXX .XXX XXXX .XXXX FRACTIONAL XX/XX ANGULAR XX°XX'		SEE SHT. 1	
MATERIAL		DRN	8 NOV88	BY	REVISION DESCRIPTION
FINISH		CHK		DATE	
		ENGR			
		PROJ			
PART NUMBER	DA21E250	QTY	1	TITLE	
COMPUTERVISION CORP.		SIGNATURE		DWG NO.	
801 BURLINGTON ROAD BEDFORD, MASS. 01730		DATE		SHT 10 OF 16 SHTS	



MEMORY CHIPS 6S THRU 6AA
AND 6F THRU 6M MAY BE
EITHER ALL 4027-3 OR
4116-3 PARTS

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION		TOLERANCES DECIMAL XX .XX XXX .XXX XXXX .XXXX FRACTIONAL 1/16 ANGLES 30°		SEE SHT. 1	
MATERIAL		DRN	8 HOURS	SYM	REVISION DESCRIPTION
FINISH		CHK		UNIT	128/32K MEMORY
		ENGR		WT.	A/B PORT SCHEM. DIAGRAM
PART NUMBER	DA21E250	QTY	1	SCALE	DWG NO. DS21E252
COMPUTERVISION CORP. 301 BURLINGTON ROAD BEDFORD, MASS. 01730			DATE	UNIT	SHT 11 OF 16 SHTS



MEMORY CHIPS 8S THRU 8AA
AND 8F THRU 8M MAY BE
EITHER ALL 4027-3 OR
4116-3 PARTS

DS21E252
E

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRO- DUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION		TOLERANCES DECIMAL XX .XX XXX .XXX XXX .XXX FRACTIONAL .XX/16 ANGULAR .XX		6EE SHT. 1	
MATERIAL		QTY	REV	DESCRIPTION	DATE
FINISH		QTY	REV	DESCRIPTION	DATE
PART NUMBER	DA21E250	1	REV	DESCRIPTION	DATE
COMPUTERVISION CORP.		SIGNATURE		DATE	
300 BURLINGTON RD. BEDFORD, MASS. 01730		UNIT		SHT 13 OF 16 SHTS	

B PORT CONNECTORS

CONN C

1	BINTR	2
3		4
5	BPORTACT	6
7		8
9		10
11	BIRST	12
13	BCLR	14
15	BIOPLS	16
17		18
18	BDS 3	20
21	BDS 2	22
23	BDS 1	24
25	BDS 0	26
27		28
29		30
31	BRQENB	32
33		34
35	BOATA 10	36
37	BOATA 1	38
38	BOATA 4	40
41	BOATA 5	42
43	BDATA 6	44
45	BDATA 7	46
47	FREE	48
49		50
	BINTPOUT	

CONN E

1		B MEM RD	2
3	B MEM RO		4
5	B MEMWRT	B MEMWRT	6
7		B LDMAR	8
9	B LDMAR		10
11	B MEM BUS 15		12
13	B MEM BUS 14		14
15	B MEM BUS 13		16
17	B MEM BUS 12		18
18	B MEM BUS 11		20
21	B MEM BUS 10		22
23	B MEM BUS 9		24
25	B MEM BUS 8		26
27	B MEM BUS 7		28
29	B MEM BUS 6		30
31	B MEM BUS 5		32
33	B MEM BUS 4		34
35	B MEM BUS 3		36
37	B MEM BUS 2	BWAD2	38
39	B MEM BUS 1	BWAD1	40
41	B MEM BUS 0	RESET	42
43	BMC 3	BWADO	44
45	BMC 2	BWCO	46
47	BMC 1	BPARER	48
49		B MEM BUSY	50

ALL UNUSED PINS GROUNDED

VOLTAGE FEEDS FOR CONNECTORS PA,PB	
+12 VOLTS	B46,A7,A8
-5 VOLTS	B81
-12 VOLTS	B71,B72
+5 VOLTS	A/B3.A/B4.A/B97.A/B98
GND	A/B1.A/B2.A/B99.A/B100

DS21E252

E

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION		TOLERANCES DECIMAL XX .XX XXX .XXX FRACTIONAL 1/64 ANGULAR .100			
MATERIAL		DIM & HOLES		SEE SHT. 1	
FINISH		ENGR		BYN	REVISION DESCRIPTION
		PROJ		DATE	
PART NUMBER	DA21E250	QTY	1	TITLE 128/32K MEMORY	
COMPUTERVISION CORP.			DWG NO. DS21E252		
301 BURLINGTON ROAD ROUTE 52			SHT 18 OF 16 SHTS		
BEFORD, MASS. 01730					

32K/128K Memory Unit
DS21E227 (Obsolete)

	<u>Sheet No.</u>
Block Diagram	
Address Selection	1
B Port Connections	1
Data Input/Output	2
Bus and MAR Logic	3
Cycle Timing Logic	4
Refresh Logic	4
Bus Control Logic	5
I/O Logic	6
Typical Rank	7
Memory Address Logic	8
Array	9

128K BOARD (DA21E225-01)

I. JUMPER INFO.
(CONNECTIONS NORMALLY MADE IN ETCH)

1. JP3
2. JP5
3. JP7
4. JPI

II. ADDRESS SELECT CHART

* FIELD #	$\overline{MC0}$	$\overline{MC1}$	CLOSED CONTACTS SWITCH PACK 1T
0, 1, 2, 3	H	H	2, 4 * *
4, 5, 6, 7	H	L	2, 3 * *
8, 9, 10, 11	L	H	1, 4 * *
12, 13, 14, 15	L	L	1, 3 * *

*.NOTE: EACH FIELD # REPRESENTS ONE 32K
SEGMENT OF MEMORY.

* * NOTE: ALL OTHER CONTACTS OPEN.

III. HARDWARE CONFIGURATION INFO.

1. MEMORY CHIPS ARE MK4116-3.
2. RESISTORS R2 & R3 ARE BOTH INSERTED.
3. ADJUST POT1 (R138) SUCH THAT TP4H-4 HAS A REPETITION RATE OF 14.5 μ S.

GENERAL NOTES :

1. UNLESS OTHERWISE SPECIFIED RESISTOR
VALUES ARE IN OHMS, $\pm 5\%$
CAPACITOR VALUES ARE IN MICROFARADS

32 K BOARD (DA21E225-02)

I. JUMPER INFO.

1. CUT CONNECTIONS JP3, JP5, JP7, JP1
2. MAKE CONNECTIONS JP2, JP4, JP6,

II. ADDRESS SELECT CHART

* FIELD #	MC0	MC1	MC2	MC3	CLOSED CONTACTS SWITCH PACK 1T
0	H	H	H	H	2, 4, 6, 8 * *
1	H	H	H	L	2, 4, 6, 7 * *
2	H	H	L	H	2, 4, 5, 8 * *
3	H	H	L	L	2, 4, 5, 7
4	H	L	H	H	2, 3, 6, 8
5	H	L	H	L	2, 3, 6, 7
6	H	L	L	H	2, 3, 5, 8
7	H	L	L	L	2, 3, 5, 7
8	L	H	H	H	1, 4, 6, 8
9	L	H	H	L	1, 4, 6, 7
10	L	H	L	H	1, 4, 5, 8
11	L	H	L	L	1, 4, 5, 7
12	L	L	H	H	1, 3, 6, 8
13	L	L	H	L	1, 3, 6, 7 * *
14	L	L	L	H	1, 3, 5, 8 * *
15	L	L	L	L	1, 3, 5, 7 * *

* NOTE: EACH FIELD # REPRESENTS ONE 32K
SEGMENT OF MEMORY.

* * NOTE: ALL OTHER CONTACTS OPEN

III. HARDWARE CONFIGURATION INFO.

1. MEMORY CHIPS ARE MK4027-3.
2. REMOVE RESISTOR R2.
3. ADJUST POT1 (R138) SUCH THAT TP4H-4 HAS REPETITION RATE OF 29 μ s.

B PORT CONNECTORS

CONN D

1	BINTPOUT	
11	BIORST	
	BCLR	
	BIOPLS	
	BINTA	
	BDS5	
21	BDS4	
	BDS3	
	BDS2	
	BDS1	
	BDS0	
31	BRQENB	
	BDATAI0	
	BDATAI1	
	BDATAI2	
41	BDATAI3	
	BDATAI4	
	BDATAI5	
49	BINTR	

CONN E

I	B MEM RD	
	B MEM WR	
	B ACCESS PROT	
	B WRT PROT	
	B MEM BUSY	
II	B MEM BUS 15	
	↑ ↑ ↓	14
		13
		12
		11
2I		10
		9
		8
		7
		6
3I		5
		4
		3
		2
	↓ ↓ ↓	1
4I	B MEM BUS 0	
	B MC 3	
	B MC 2	
	B MC 1	B PARITY E
49	B MC 0	BLD MAR


ALL UNUSED PINS GROUNDED

VOLTAGE FEEDS FOR CONNECTORS PA, PB

+12 VOLTS	B46, A7, A8
-5 VOLTS	B81 A5, A6
-12 VOLTS	B71, B72
+5 VOLTS	A/B3, A/B4, A/B97, A/B98
GND	A/B1, A/B2, A/B99, A/B100

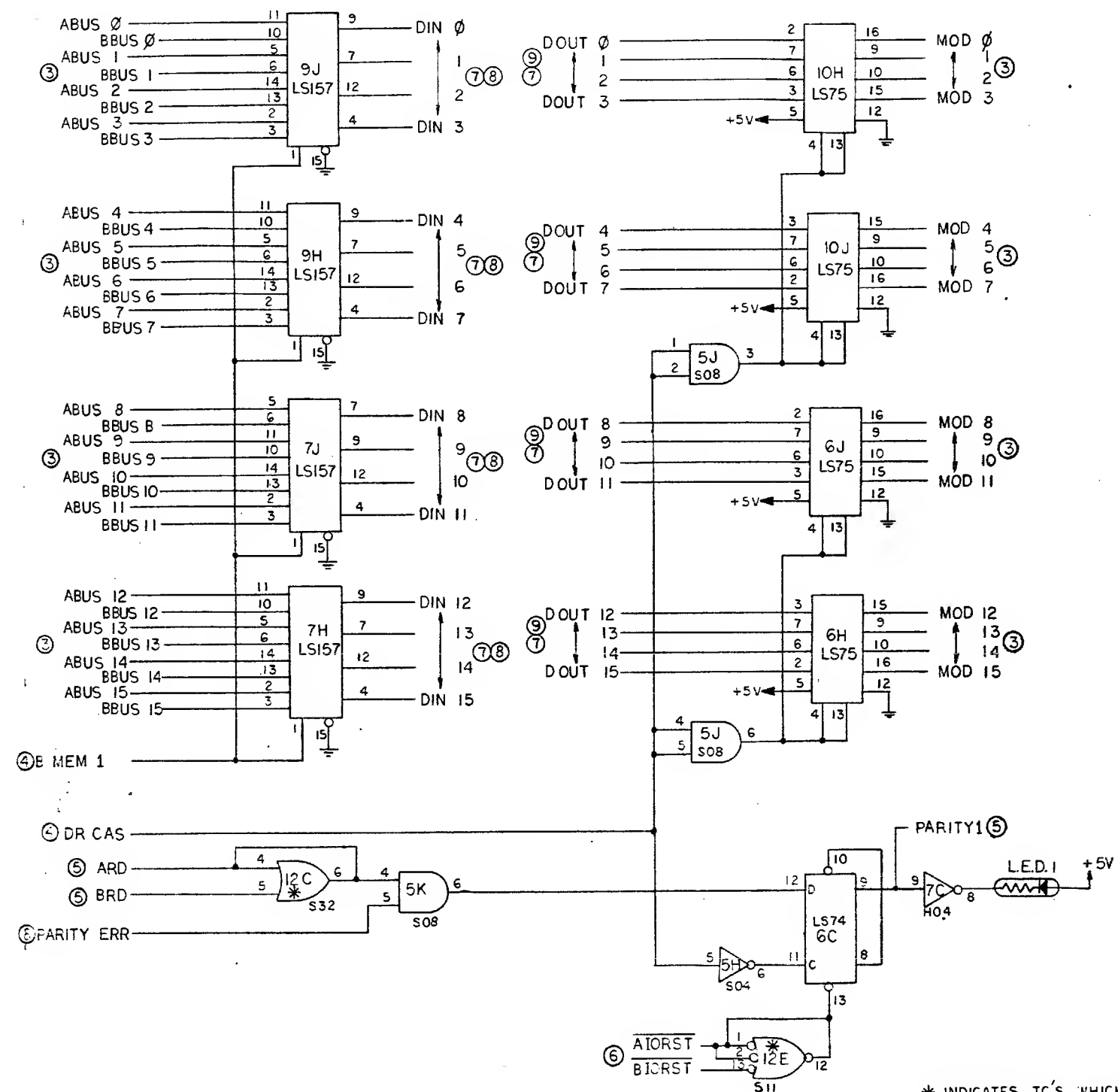
DS2IE227

GND	A/B1, A/B2, A/B99, A/B100
-----	---------------------------



see drawing DA 21E250

[illegible]



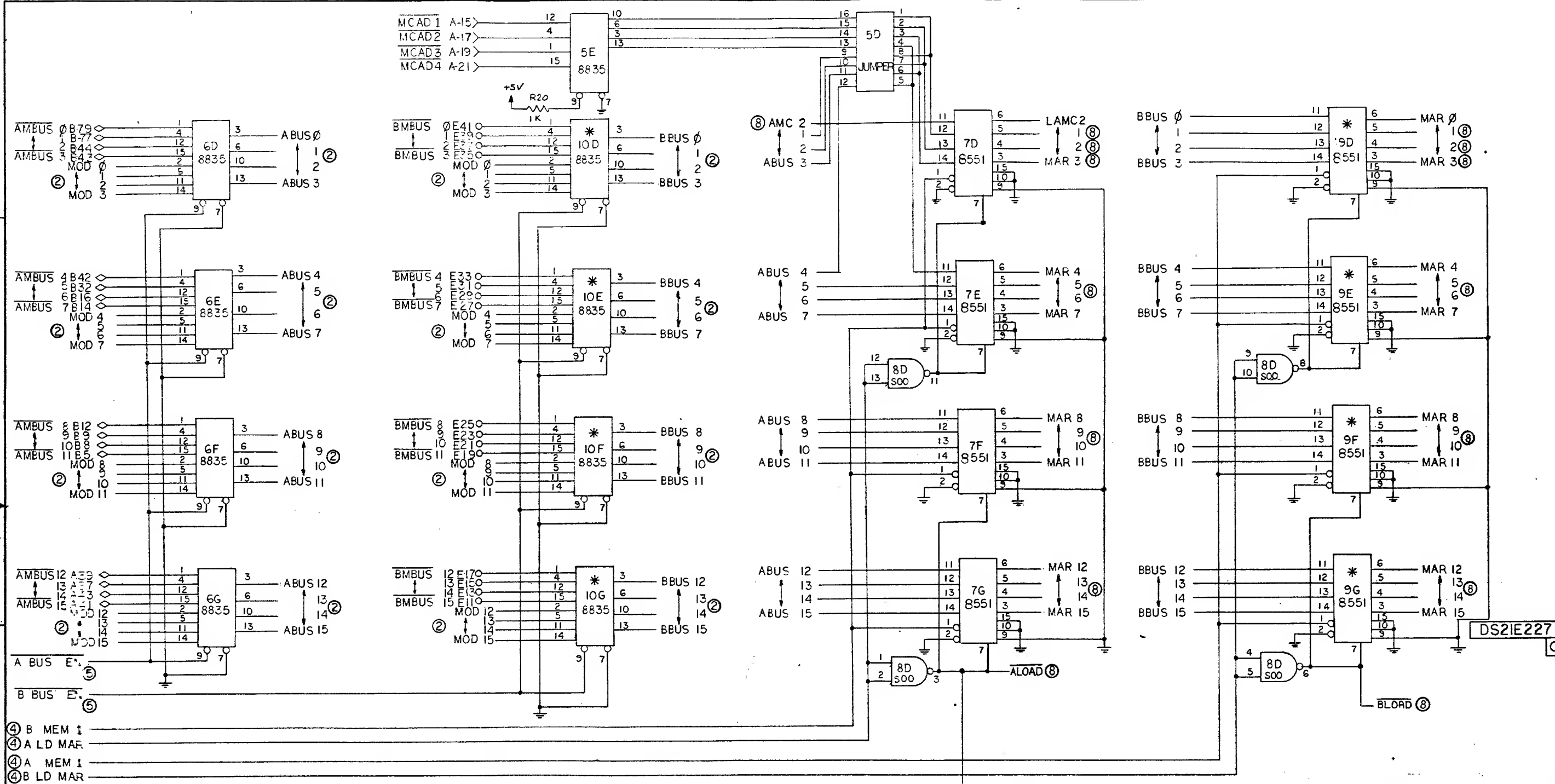
* INDICATES IC'S WHICH CAN BE REMOVED TO DISABLE B PORT LOGIC.

DATA INPUT/OUTPUT LOGIC

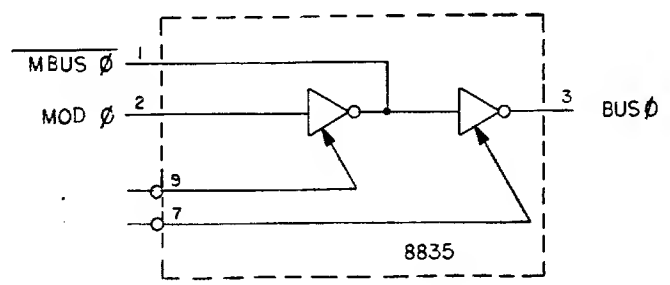
THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.		TOLERANCES X.XX DECIMAL X.XX ± .01 X.XX ± .010 FRACTIONAL ± .005 ANGULAR ± .000		SEE SH. 1	
MATERIAL:		DATE: 11/1/78		SYN: 11/1/78	
DESIGN:		CHK: 11/1/78		REV: 11/1/78	
ENGR: 11/1/78		PROJ: 11/1/78		SCALE: 11/1/78	
PART NUMBER		NEXT ASSEMBLY		QTY	
COMPUTERVISION CORP.		SOUTH AVENUE		BURLINGTON, MASS. 01803	
SIGNATURE		DATE		UNIT	
REMOVE ALL BURNS AND SHARP EDGES		SCALE		SHEET 2 OF 9	

DS2IE227

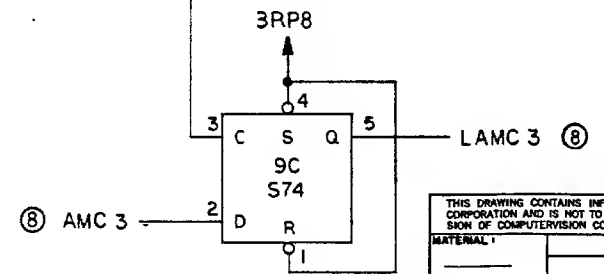
C



- ④ B MEM 1
- ④ A LD MAR
- ④ A MEM 1
- ④ B LD MAR



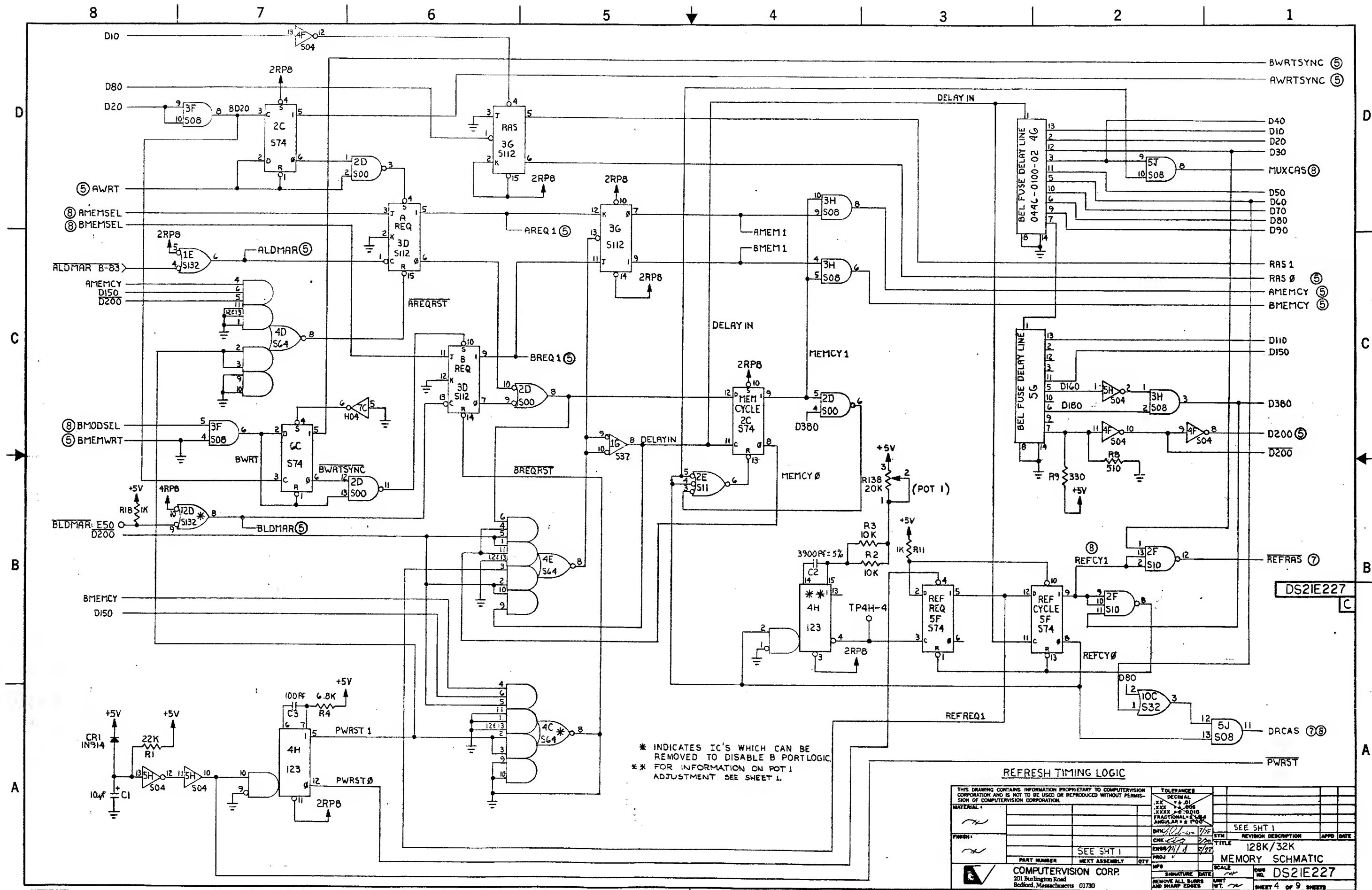
5D JUMPER PLUG	
MUC OPERATION	1, 16 2, 15 3, 14 4, 13
NON MUC OPERATION	5, 12 6, 11 7, 10 8, 9

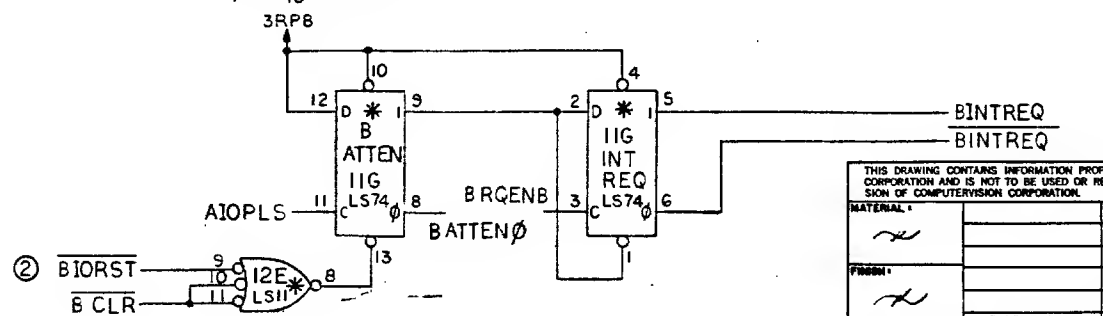
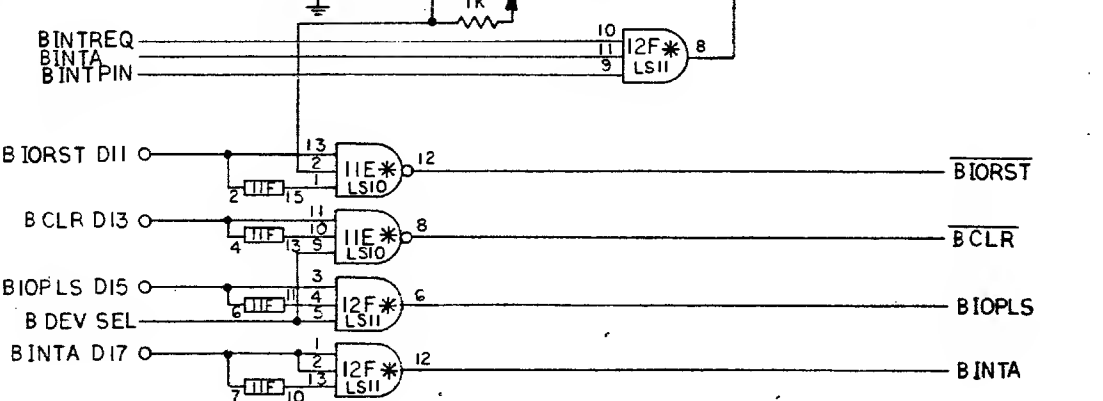
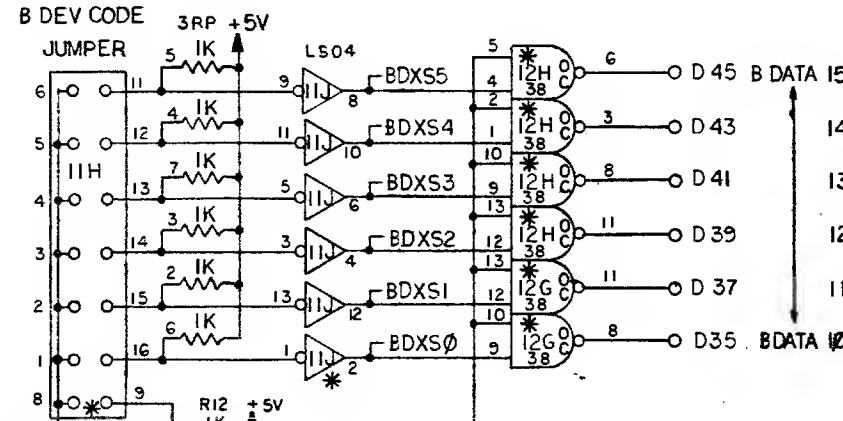
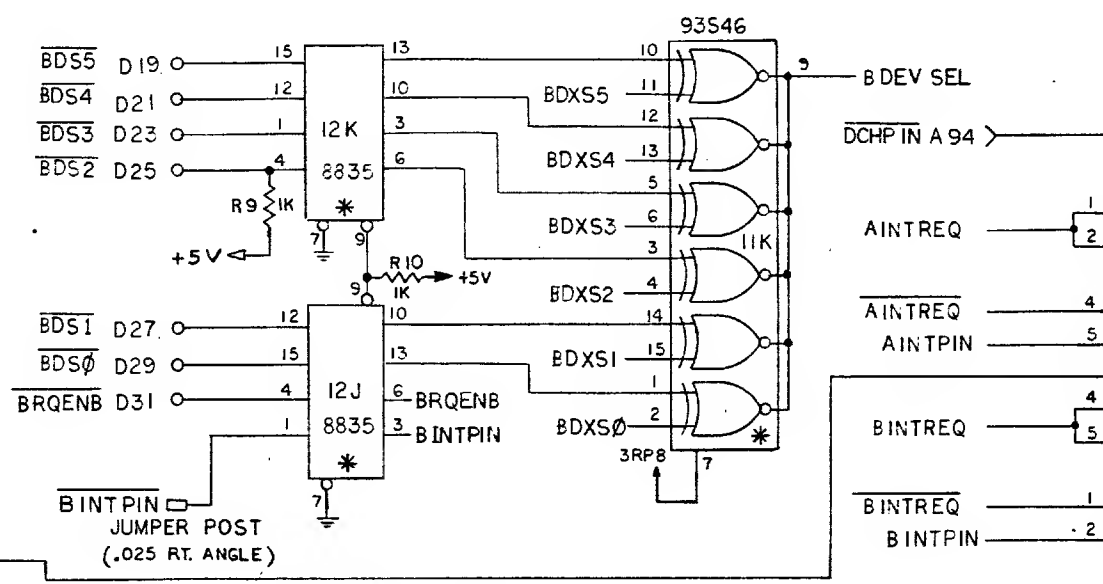
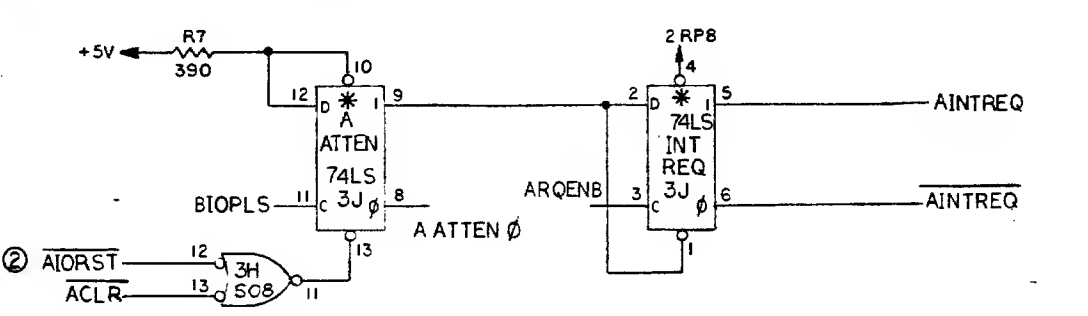
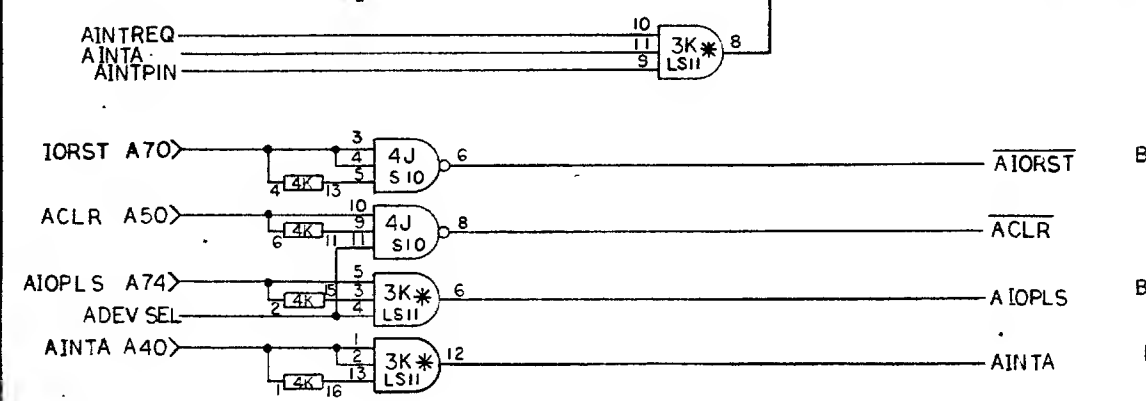
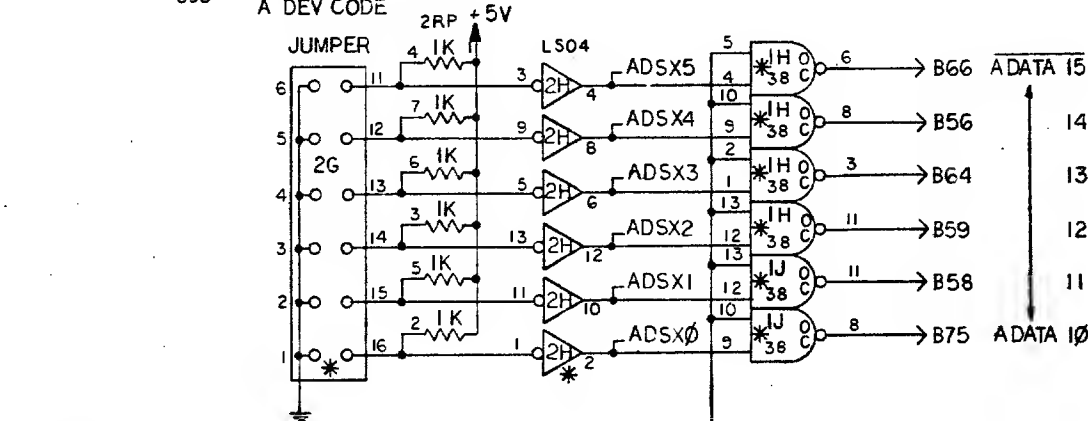
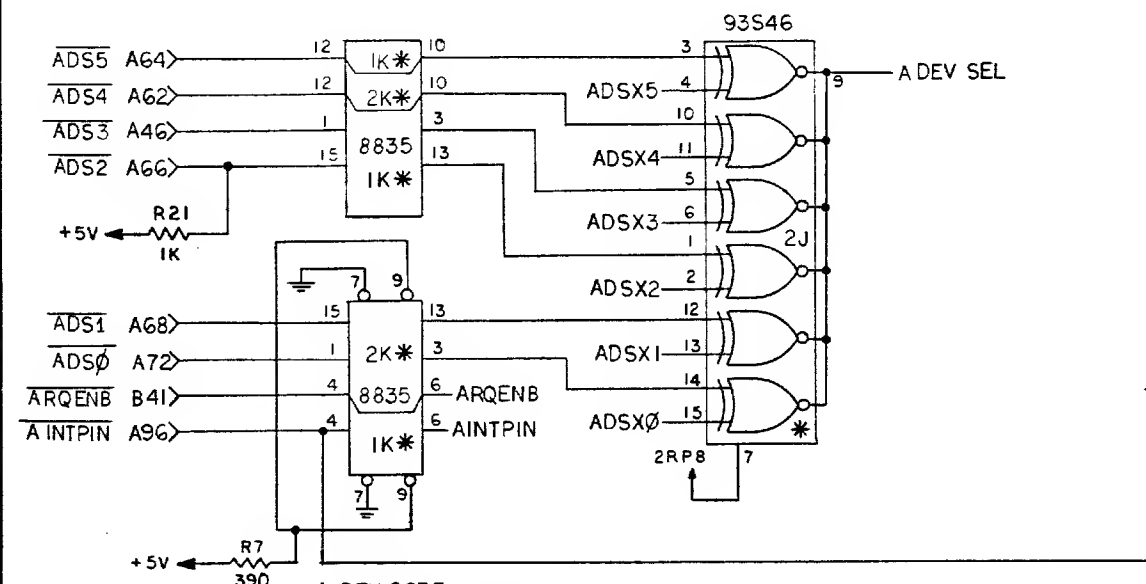


* INDICATES IC'S WHICH CAN BE REMOVED TO DISABLE B PORT LOGIC.

BUS & MAR LOGIC

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISS- SION OF COMPUTERVISION CORPORATION.		TOLERANCES DECIMAL XX .XX ± .01 XXX .XXX ± .005 XXXX .XXXX ± .010 FRACTIONAL ANGULAR ± 1°00'	
MATERIAL		DRN	DATE
FRESH		CHK	DATE
		ENGR	DATE
		PROJ	DATE
PART NUMBER	SEE SHT 1	QTY	
COMPUTERVISION CORP. SOUTH AVENUE BURLINGTON, MASS. 01803		SIGNATURE	DATE
REMOVE ALL BURRS AND SHARP EDGES		APPT	WT.
TITLE 128K/32K MEMORY SCHEMATIC		DWS NO. DS2IE227	
SHEET 3 OF 9 SHEETS			





NOTE:

INSERT ALL JUMPERS IN "A DEV CODE JUMPER BLOCK" AND "B DEV CODE JUMPER BLOCK" WHEN NOT USING B PORT.

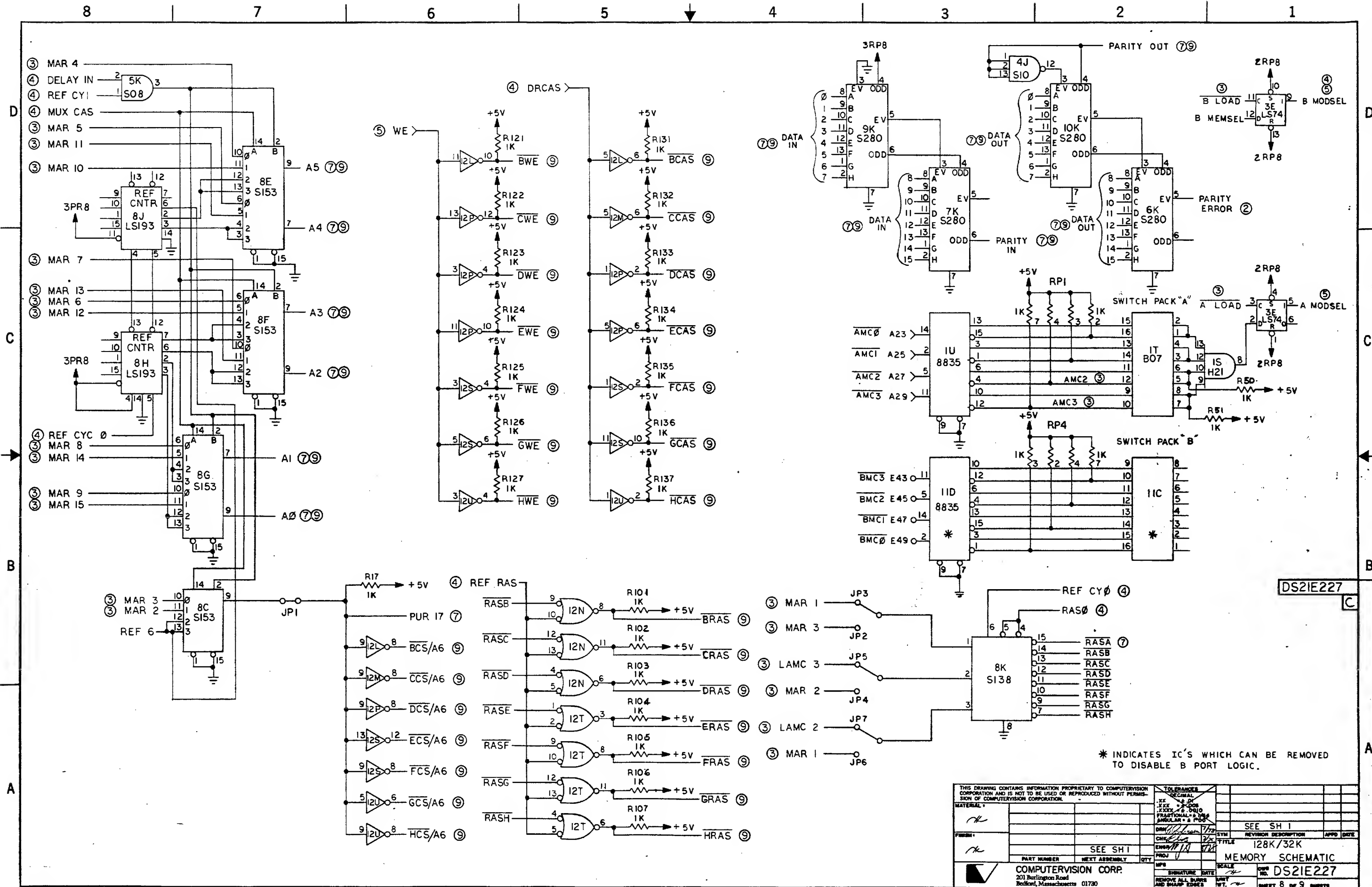
* INDICATES IC'S WHICH CAN BE REMOVED TO DISABLE B PORT LOGIC.

4K & 11K ARE RC FILTERS CONNECTED AS FOLLOWS:

DS21E227

100 P_F

I/O LOGIC			
THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.	TOLERANCES	DECIMAL	
	XXX	± 0.01	
	XXXX	± 0.005	
	XXXXX	± 0.001	
	FRACTIONAL	± 0.001	
	ANGULAR	± 0.001	
	DRY	± 0.001	
	CHK	± 0.001	
	ENG	± 0.001	
	PROJ	± 0.001	
	SCALE	NONE	
	SIGNATURE	DATE	
	REMOVE ALL BARRIERS AND SHARP EDGES	W.T.	
PART NUMBER	NEXT ASSEMBLY	QTY	
COMPUTERVISION CORP.			
SOUTH AVENUE			
BURLINGTON, MASS. 01803			
SEE SHT 1		TITLE	
SEE SHT 1		128K/32K	
SEE SHT 1		MEMORY SCHEMATIC	
SEE SHT 1		DS21E227	
SEE SHT 1		SHEET 6 OF 9 SHEETS	

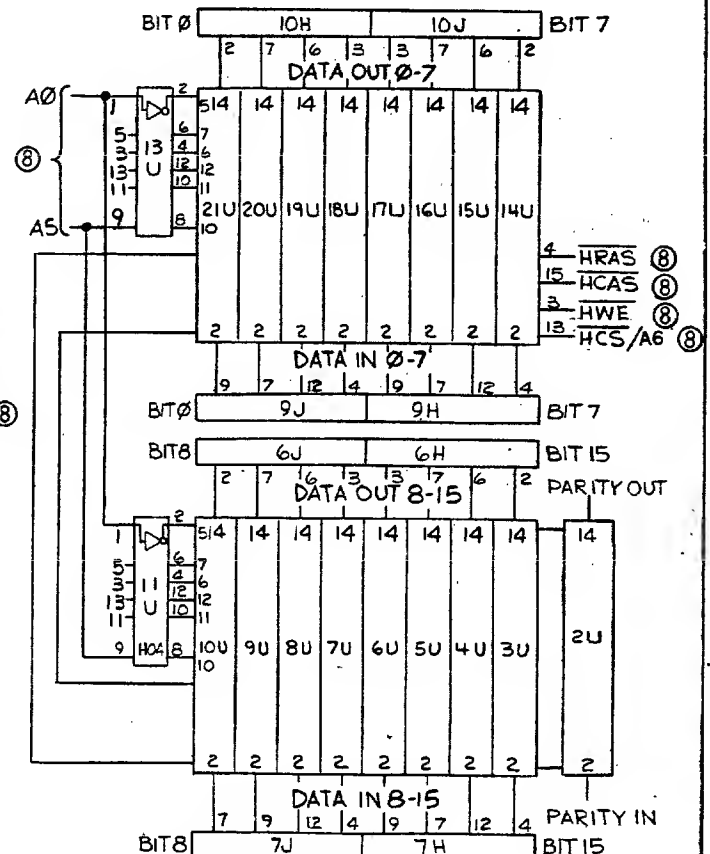
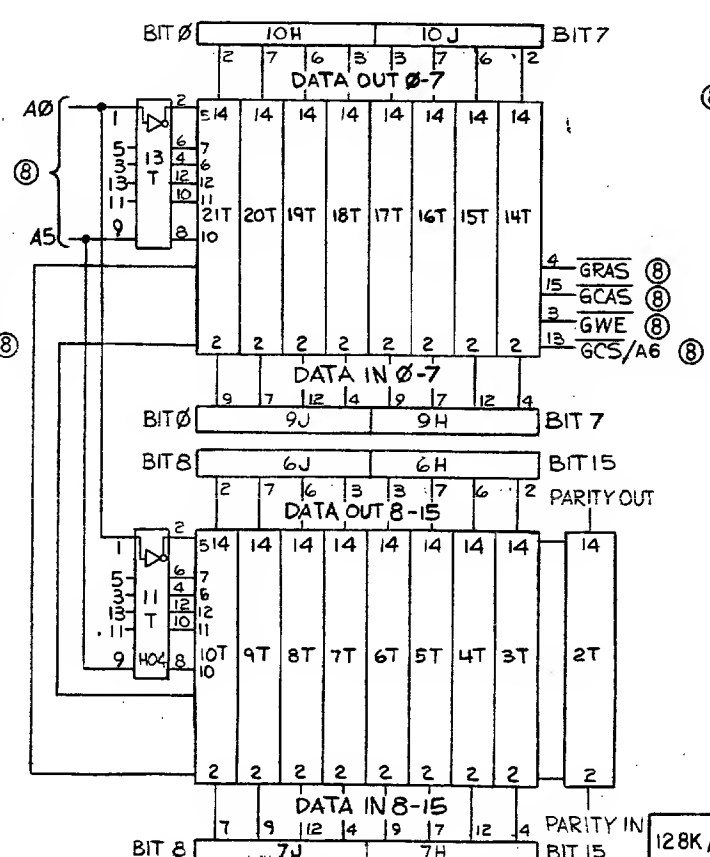
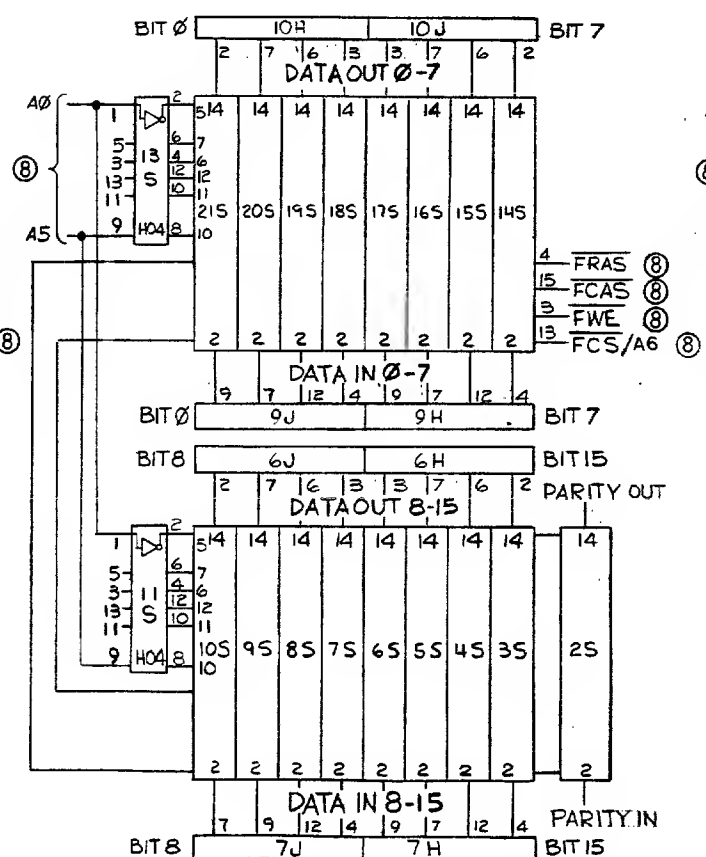
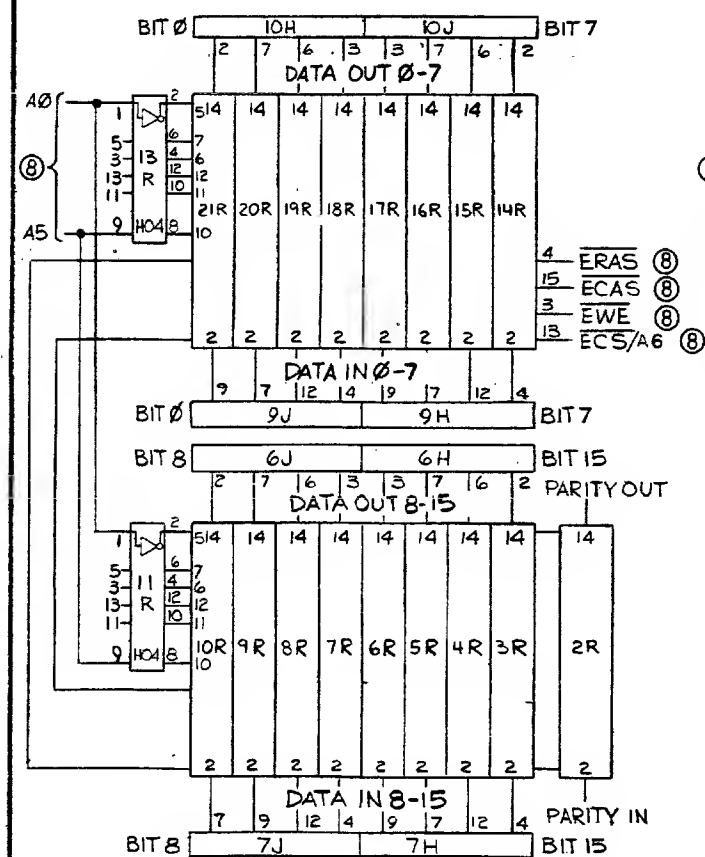
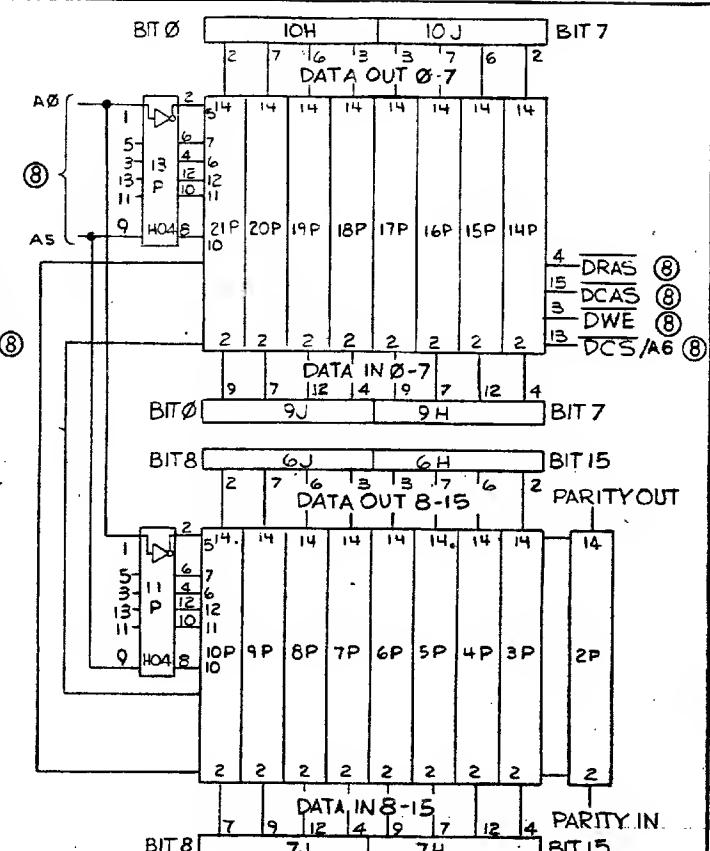
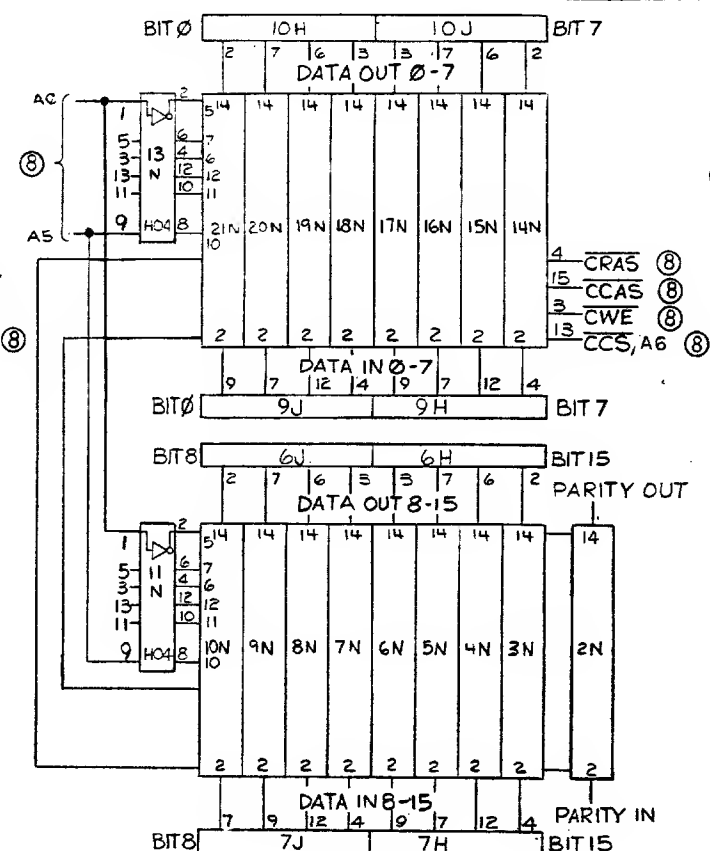
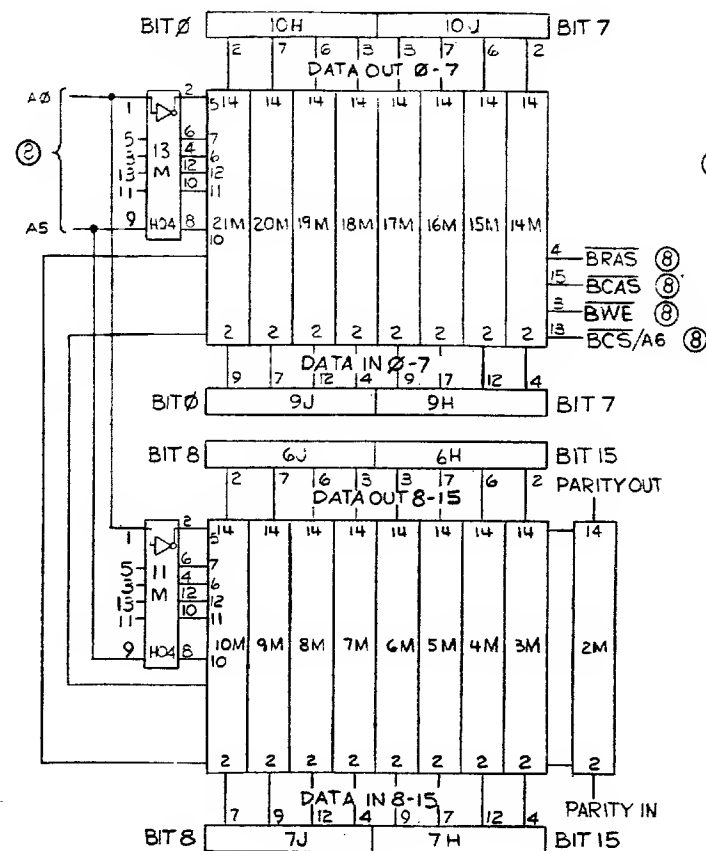


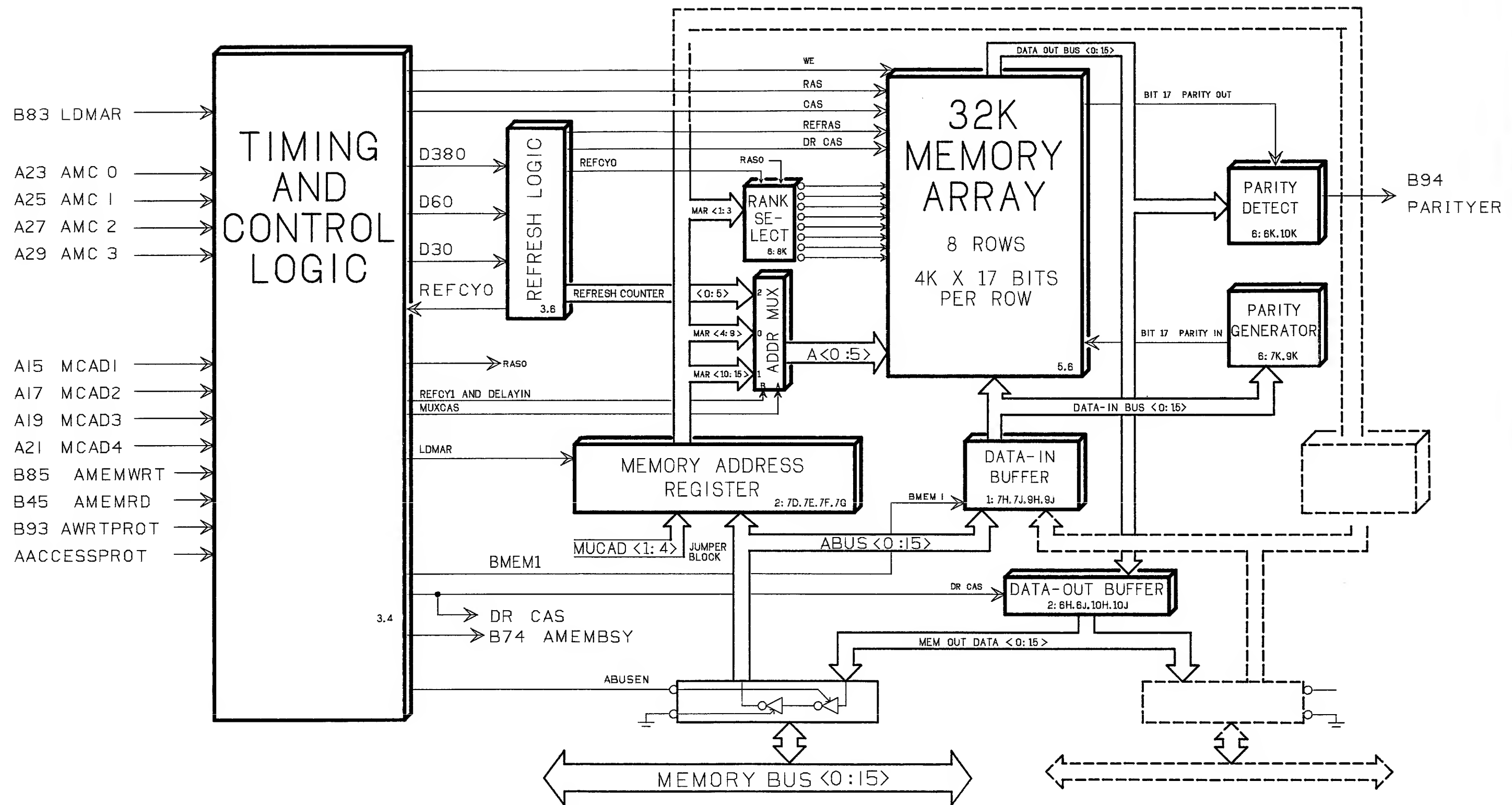
MEMORY ARRAY

FOR MORE DETAIL OF TYPICAL
MEMORY SEE SHEET 7
FOR MEMORY DATA INPUT/OUTPUT
INTERCONNECTIONS, SEE SHEET 2

NOTE:

ALL PWR. PINS ON 4027-3 OR 4116-3 ARE:
+5V PIN 9
-5V PIN 1
GND PIN 16
+12V PIN 8





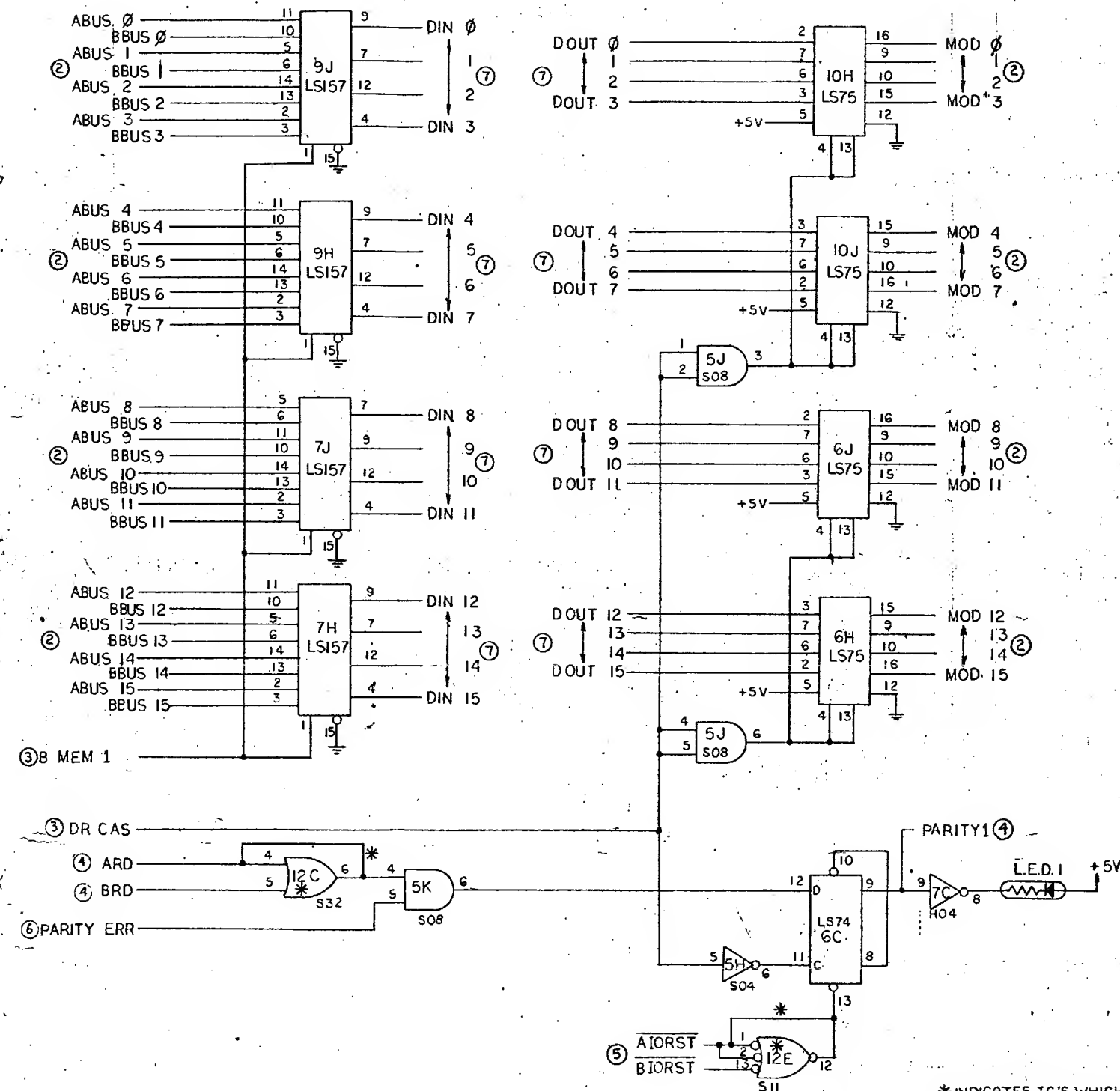
* ABUS <0.5:15> IF MAPPED; ABUS <0:15> IF UNMAPPED

DASHED LINES INDICATE B PORT

32K Memory Unit (Single Port)
DS21E102 (Obsolete)

	<u>Sheet No.</u>
Block Diagram	
Data Input/Output Logic	1
Bus and Memory Address Logic	2
Refresh Timing Logic	3
Bus Control Logic	4
I/O Logic	5
Typical Memory Rank	6
Parity Logic	6
Memory Array	7

B PORT CONNECTORS



CONN D

1'	BINTPOUT	
11	BIORST	
	BCLR	
	BIOPLS	
	BINTA	
	BDS5	
21	BDS4	
	BDS3	
	BDS2	
	BDS1	
	BDS0	
31	BRQENB	
	BDATA10	
	BDATA11	
	BDATA12	
41	BDATA13	
	BDATA14	
	BDATA15	
49	BINTR	

CONN E

I	B MEM RD	
	B MEM WRT	
	BACCESS PROT	
	B WRT PROT	
	B MEM BUSY	
II	B MEM BUS	15
		14
		13
		12
		11
2I		10
		9
		8
		7
		6
3I		5
		4
		3
		2
		1
4I	B MEM BUS	0
	BMC3	
	BMC2	
	BMC1	BPARITY ER
49	BMC0	RID MAR

ALL UNUSED PINS GRDED

VOLTAGE FEEDS FOR CONNECTORS PA, PB	
+12 VOLTS	B4C, A7, A8
-5 VOLTS	B18
-12 VOLTS	B7I, B72
+5 VOLTS	A/B3, A/B4, A/B97, A/B98
GROUND	A/B1, A/B2, A/B99, A/B100

DS21E102


DS 21 E 102 Rev D
1077 added

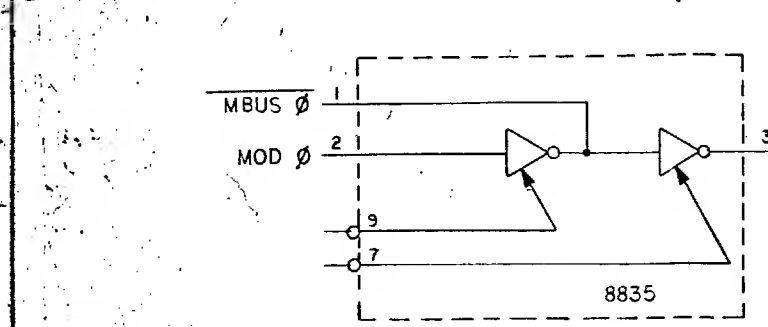
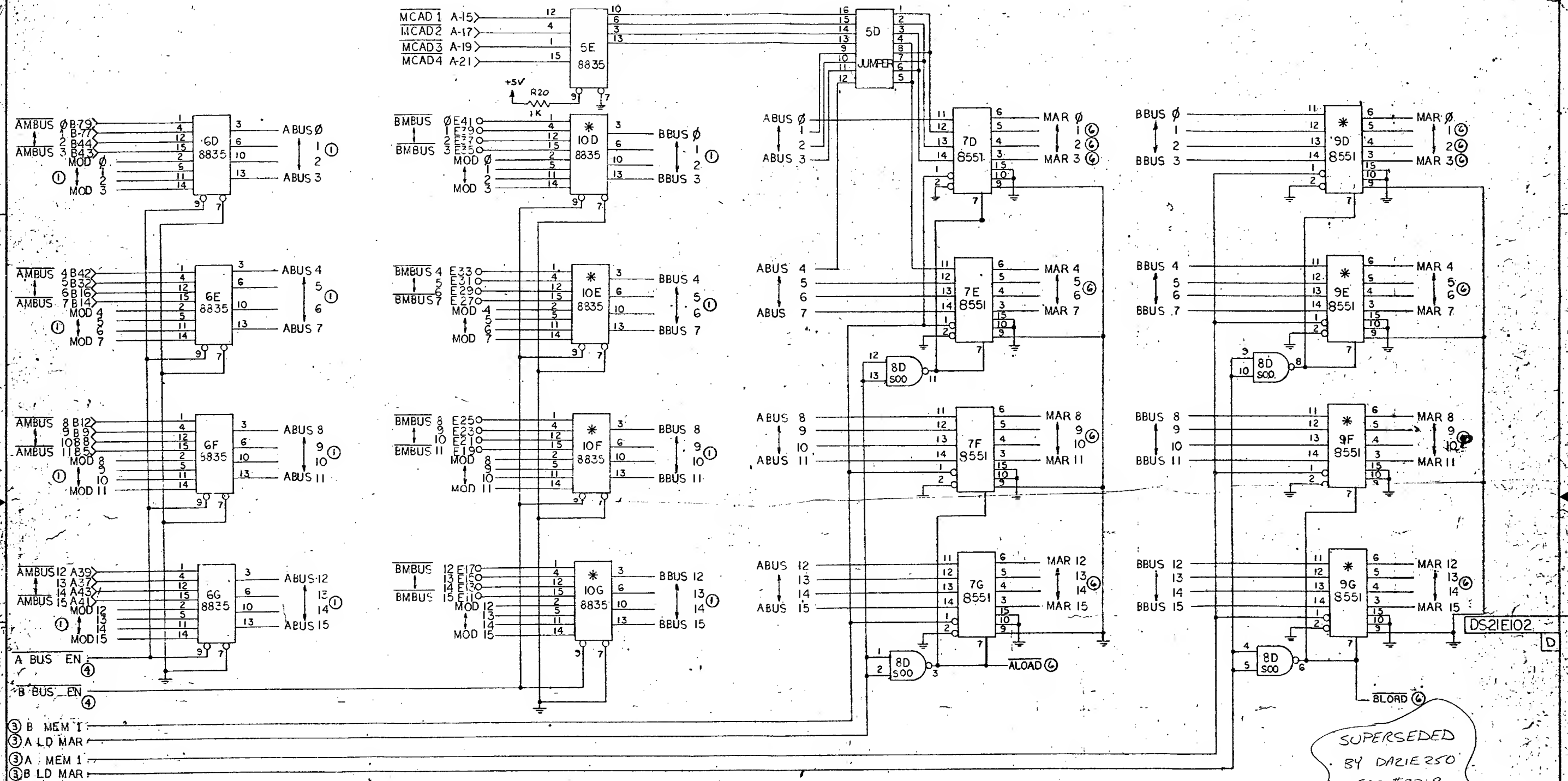
SUPERSEDED
BY DARIER50
ECO #3318
1/9/80
D. Stuart

DATA INPUT /

DATA INPUT / OUTPUT LOGIC

*INDICATES IC'S WHICH CAN BE REMOVED AND CONNECTIONS WHICH CAN BE ADDED TO DISABLE B PORT LOGIC.

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.				TOLERANCES DECIMAL .XX ± .005 .XXX ± .010 .XXXX ± .015 FRACTIONAL ± .005 ANGULAR ± 1°00'				D ECO # 2934 C2 ECO # 2729 B2 ECO # 2682 1/2 REL ECO # 2595				1-21-78 1-21-78 1-21-78 1-21-78			
MATERIAL:								DRN T.R. Bono 1/2% OKK T. 7/4 ENGR. 1/15 PROJ. 1/22				TITLE 32K MEMORY (SINGLE SCHEMATIC PORT)			
FMSB#				L21E009				REV				ESYM REVISION DESCRIPTION APPD DATE			
				D21E100				QTY							
PART NUMBER				NEXT ASSEMBLY											
 COMPUTERVISION CORP. SOUTH AVENUE BURLINGTON, MASS. 01803												SCALE NONE DWS NO. D521E102 SHEET 1 OF 7 SHEETS			



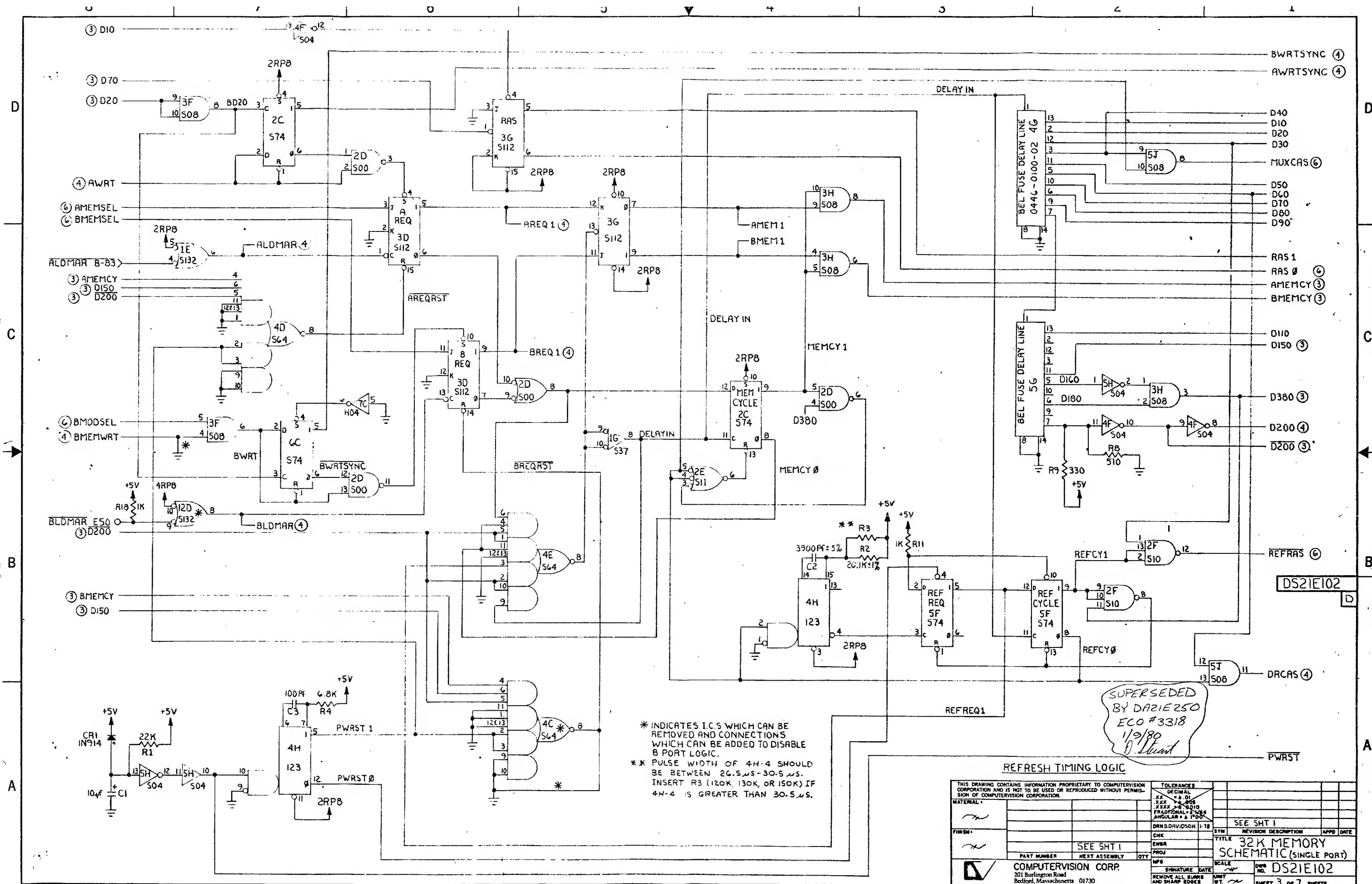
5D JUMPER PLUG	
MUC OPERATION	1, 16 2, 15 3, 14 4, 13
NON MUC OPERATION	5, 12 6, 11 7, 10 8, 9

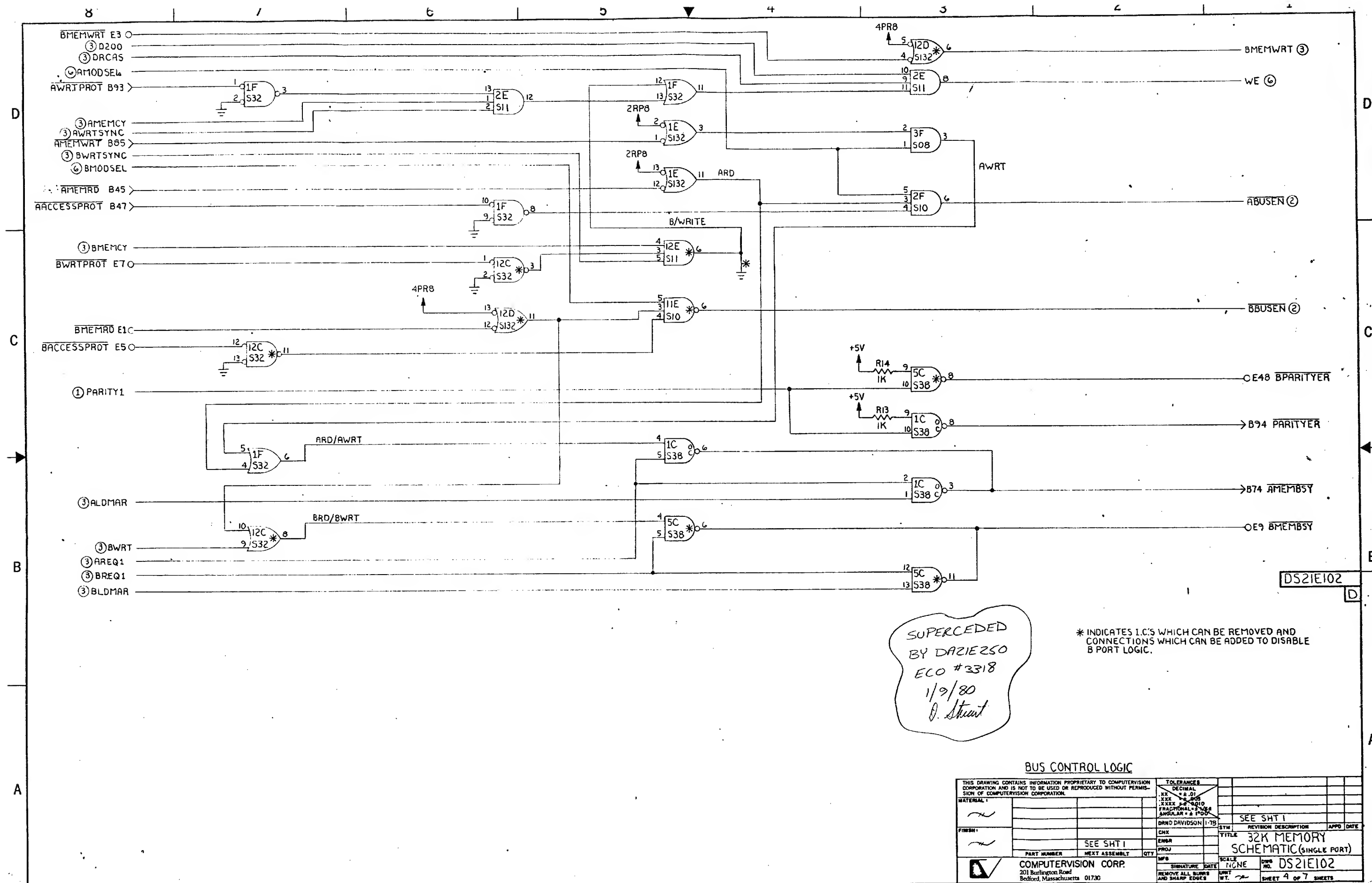
* INDICATES IC'S WHICH CAN BE REMOVED AND CONNECTIONS WHICH CAN BE ADDED TO DISABLE B PORT LOGIC.

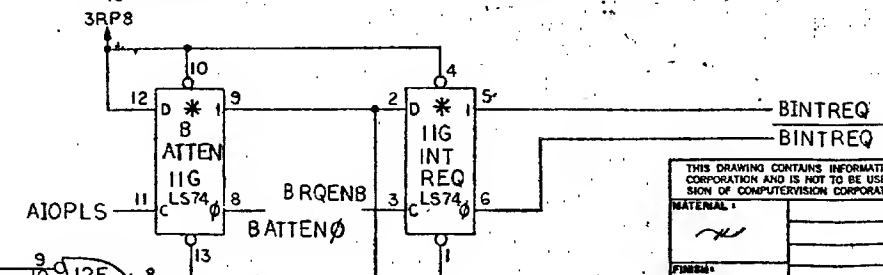
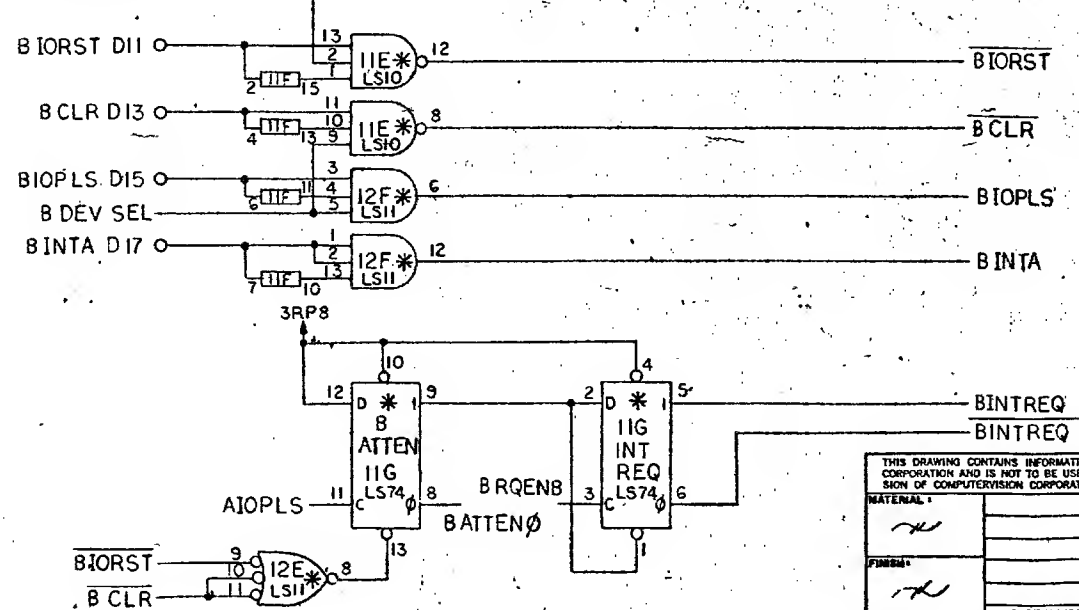
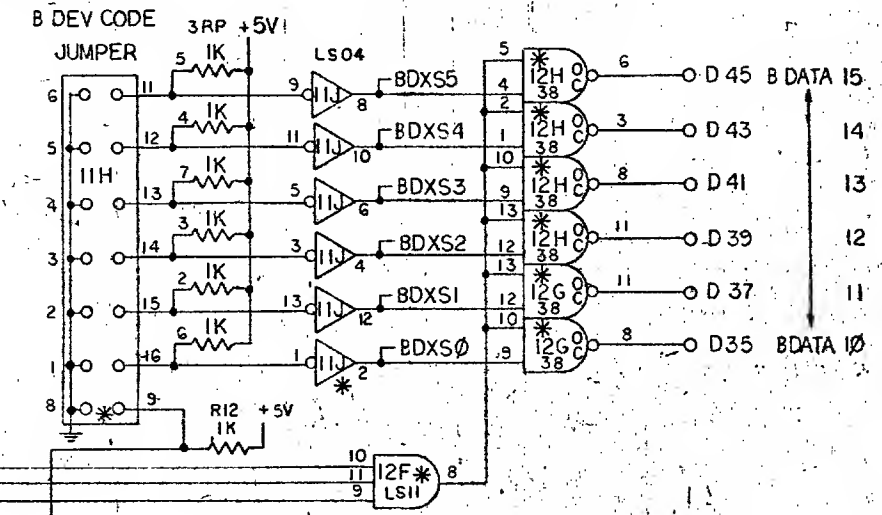
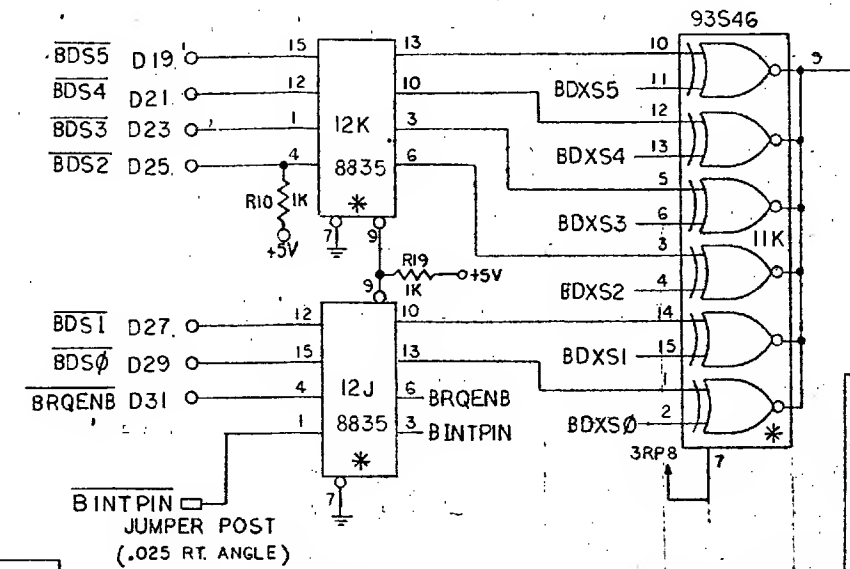
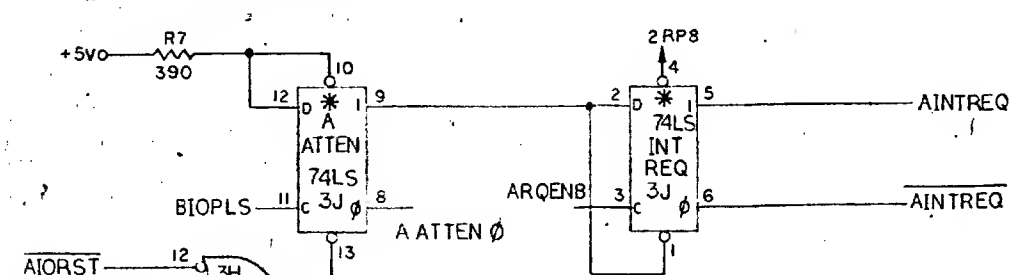
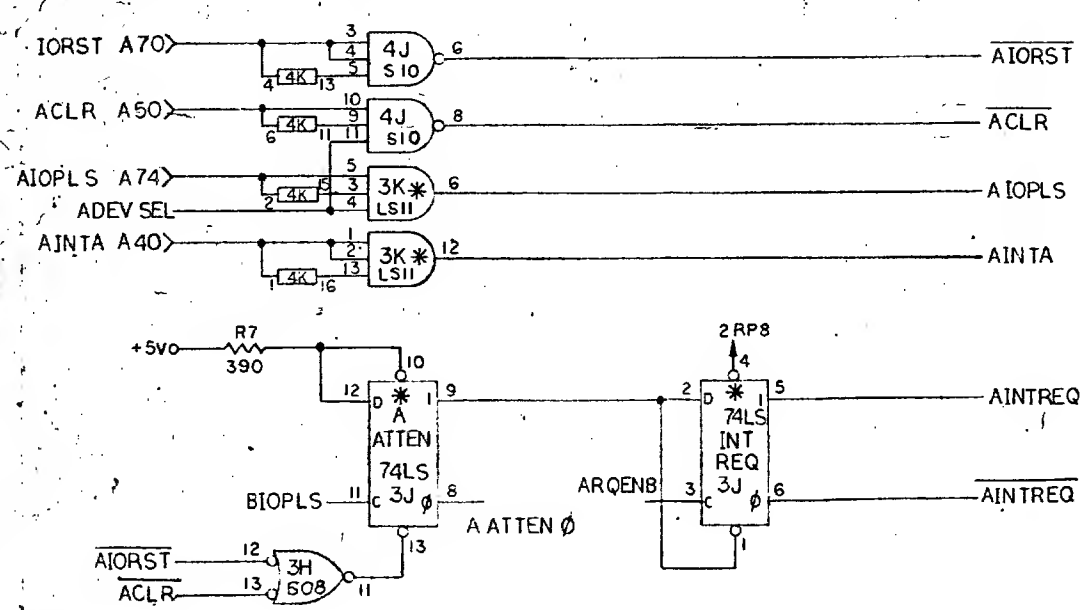
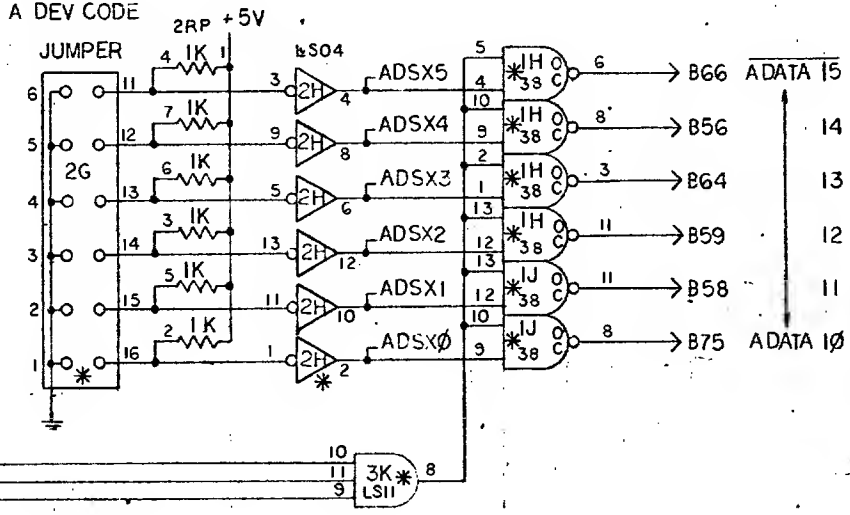
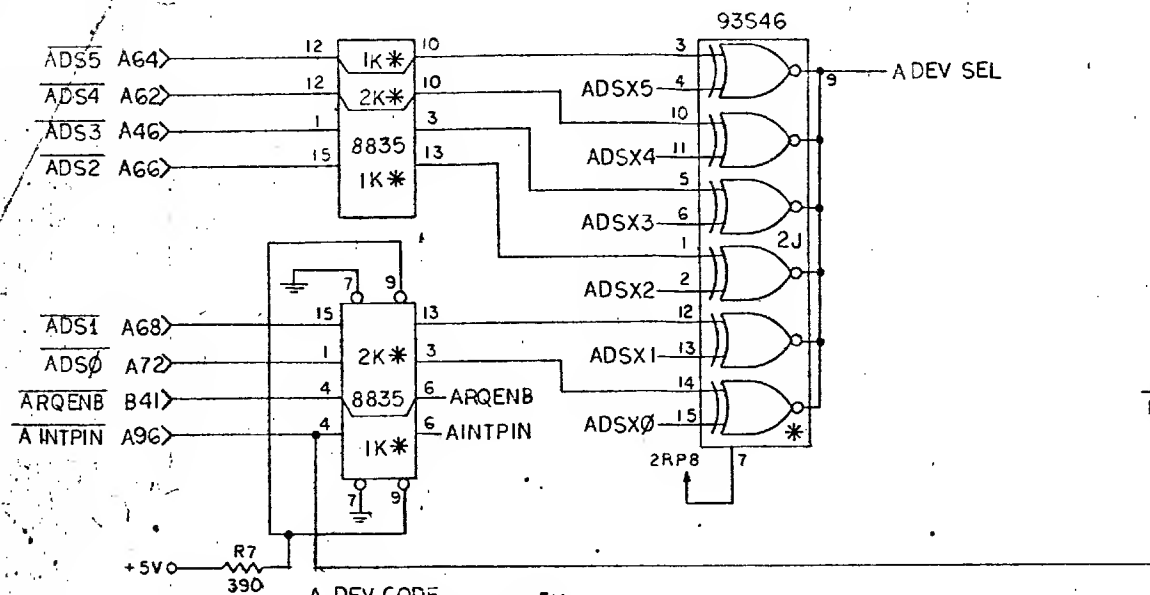
SUPERSEDED
BY DAZIER 250
ECO #3318
1/9/80
D. Atwood

BUS & MAR LOGIC

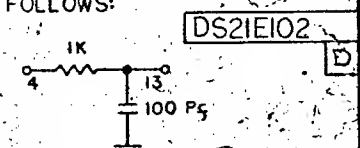
THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.		TOLERANCES DECIMAL XXX ± .01 XXX ± .005 FRACTIONAL ± .005 ANGULAR ± .005		REVISION DESCRIPTION		APPD DATE
MATERIAL		FINISH		SEE SHT 1		32K MEMORY (SINGLE SCHEMATIC PORT)
PART NUMBER		NEXT ASSEMBLY		QTY		NO. DS21E102
COMPUTERVISION CORP. SOUTH AVENUE BURLINGTON, MASS. 01803		SIGNATURE		DATE		SCALE NONE SHEET 2 OF 7 SHEETS





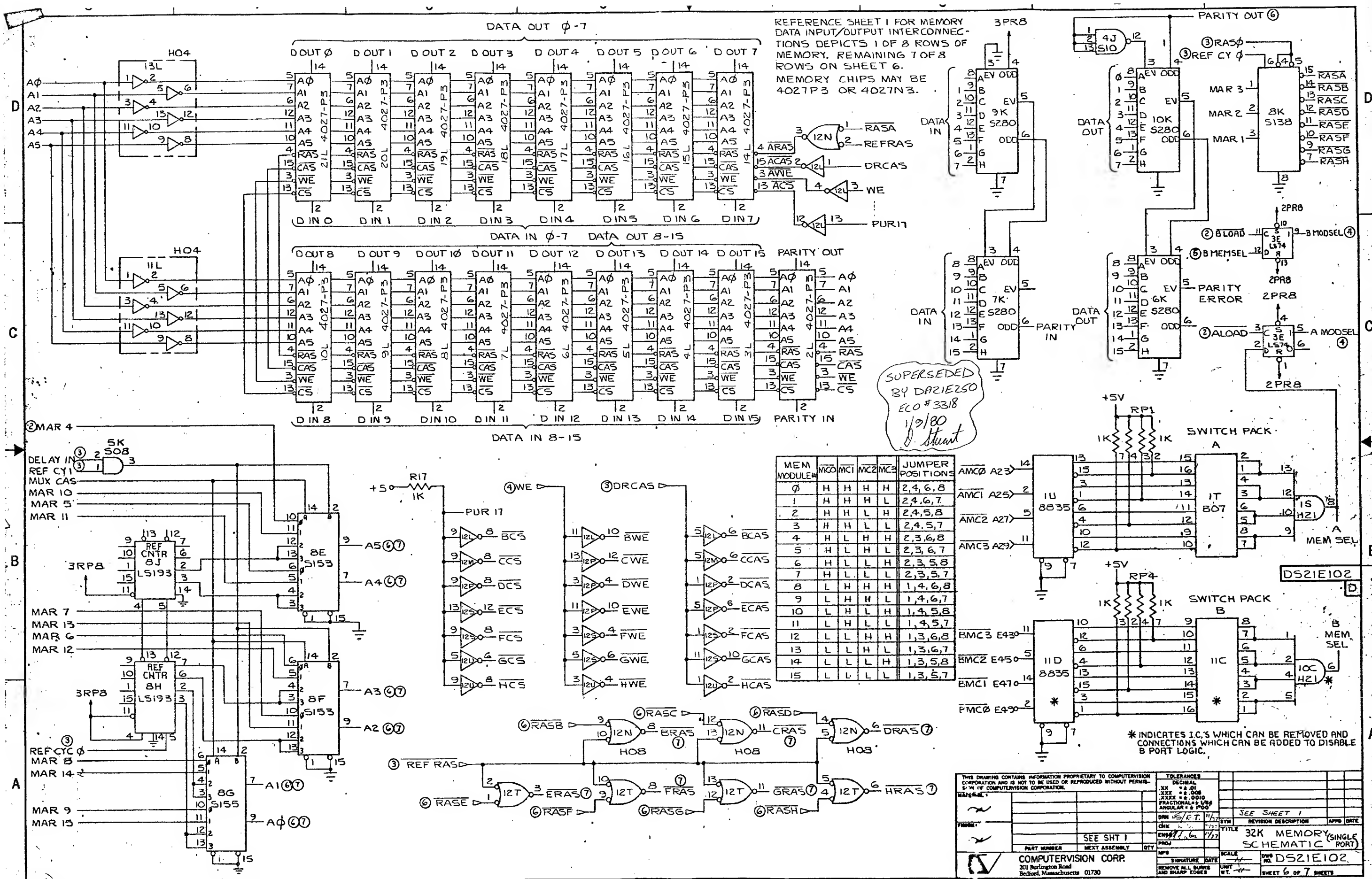


NOTE:
 INSERT ALL JUMPERS IN "A DEV CODE JUMPER BLOCK" AND "B DEV CODE JUMPER BLOCK" WHEN NOT USING B PORT.
 * INDICATES I.C.'S WHICH CAN BE REMOVED AND CONNECTIONS WHICH CAN BE ADDED TO DISABLE B PORT LOGIC.
 4K&1F ARE RC FILTERS CONNECTED AS FOLLOWS:



SUPERSEDED
 BY DAZIER25C
 ECO #3318
 1/9/80
 J. Hunt

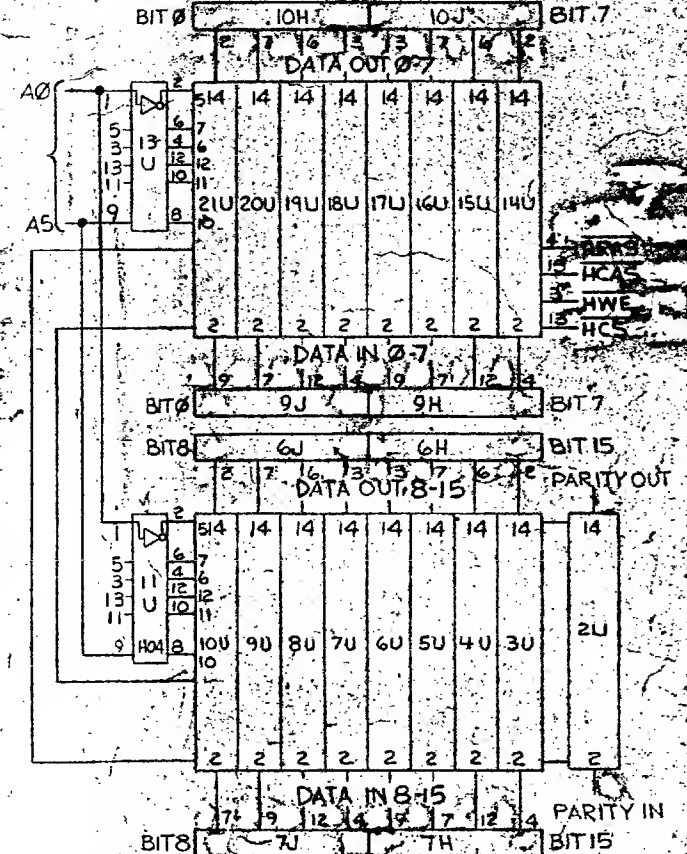
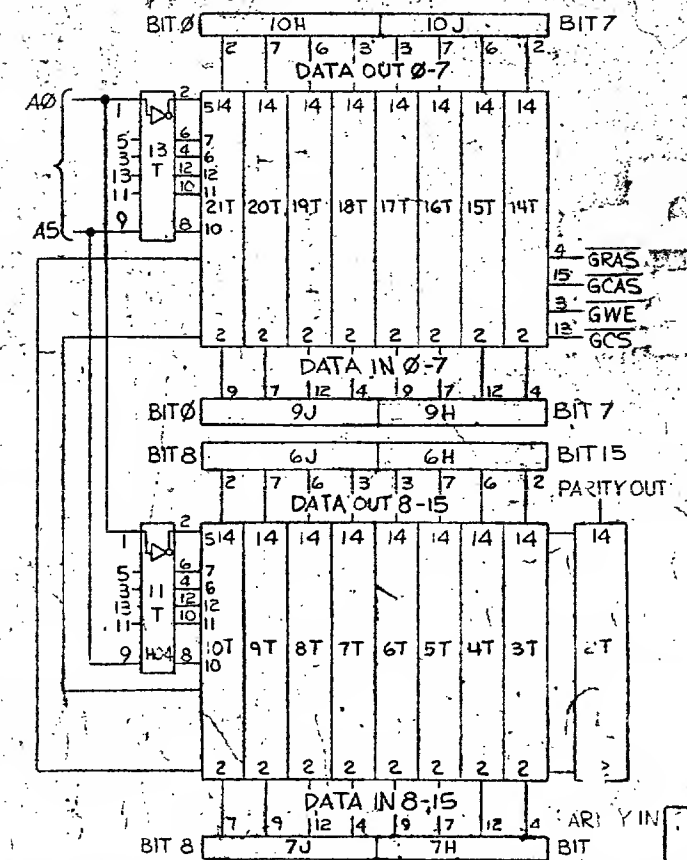
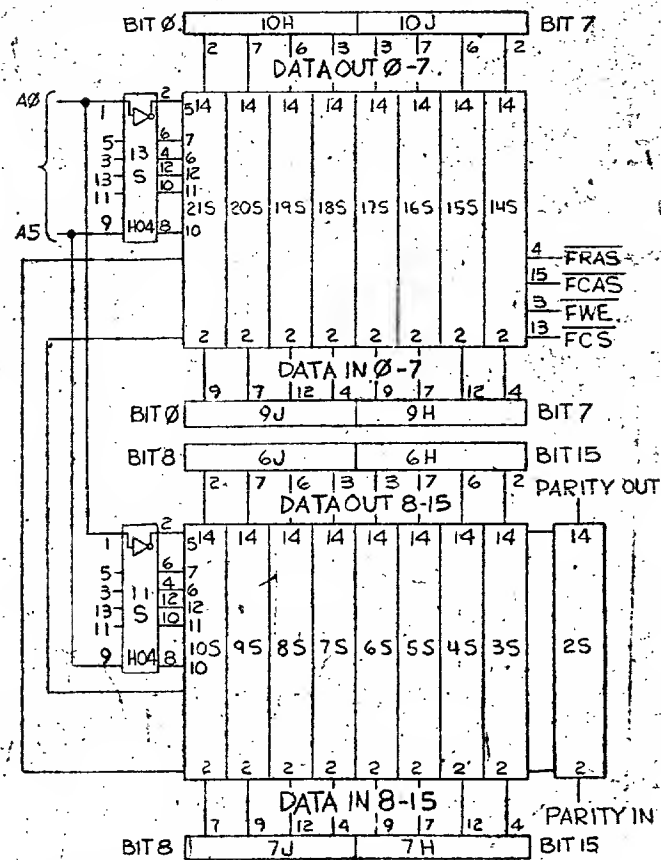
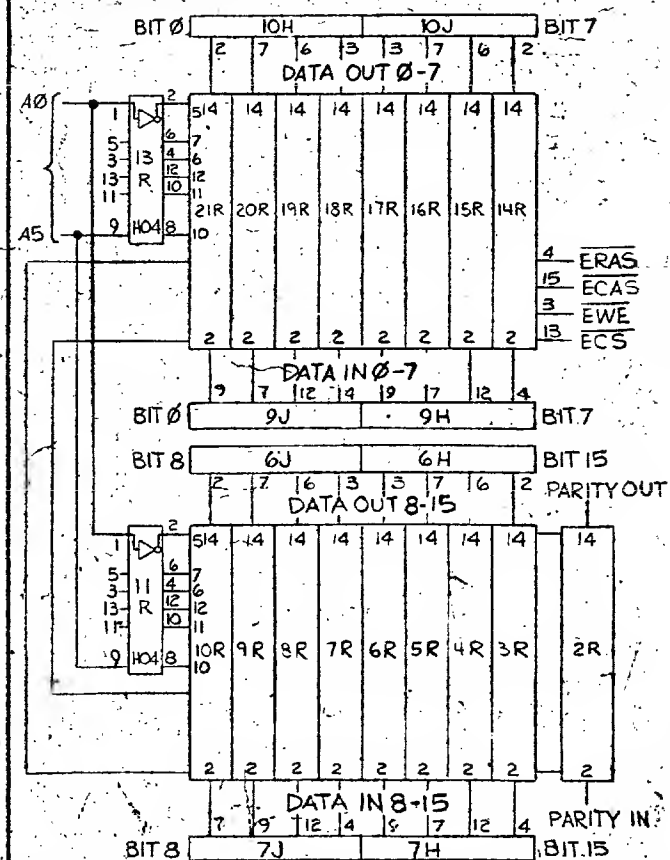
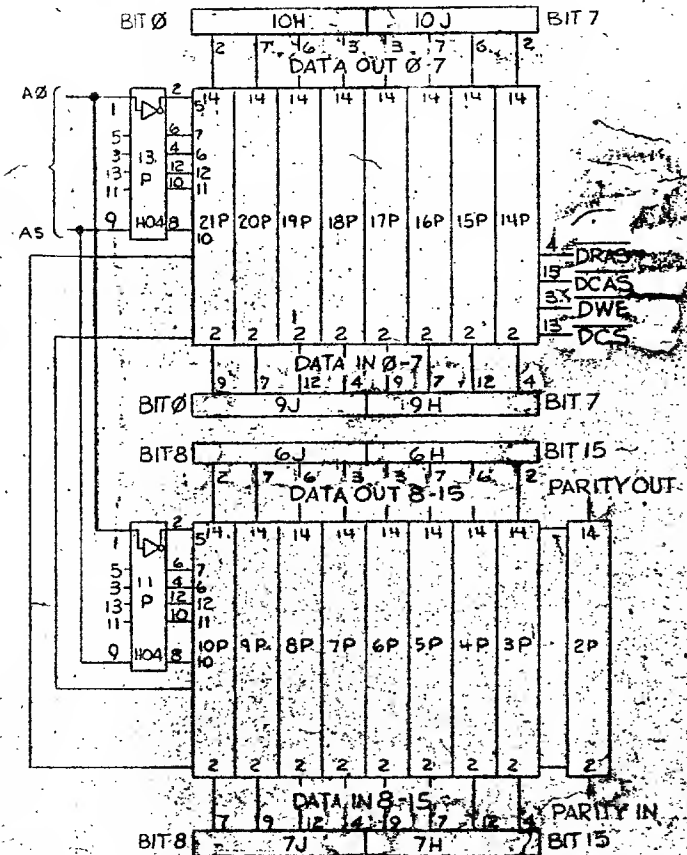
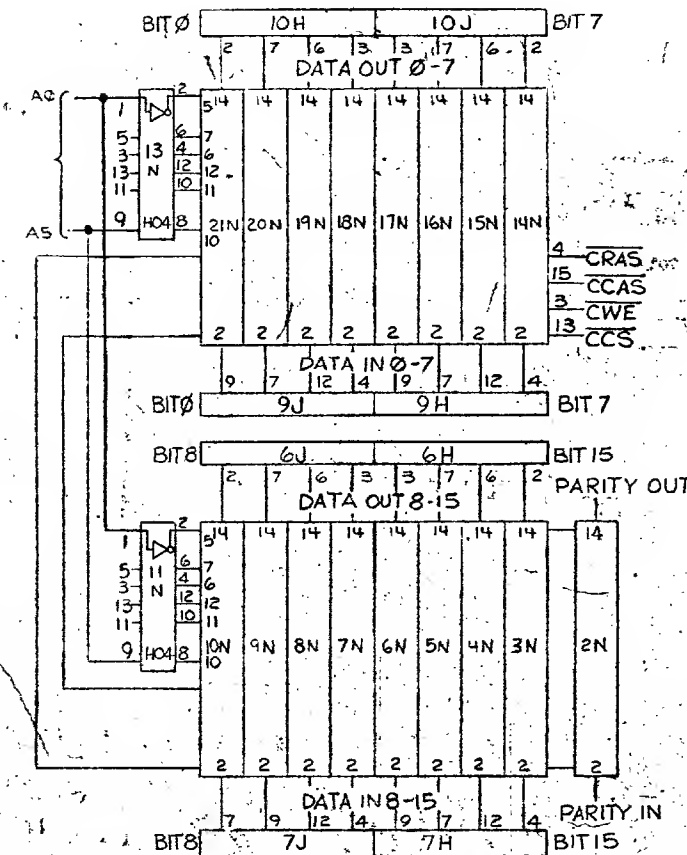
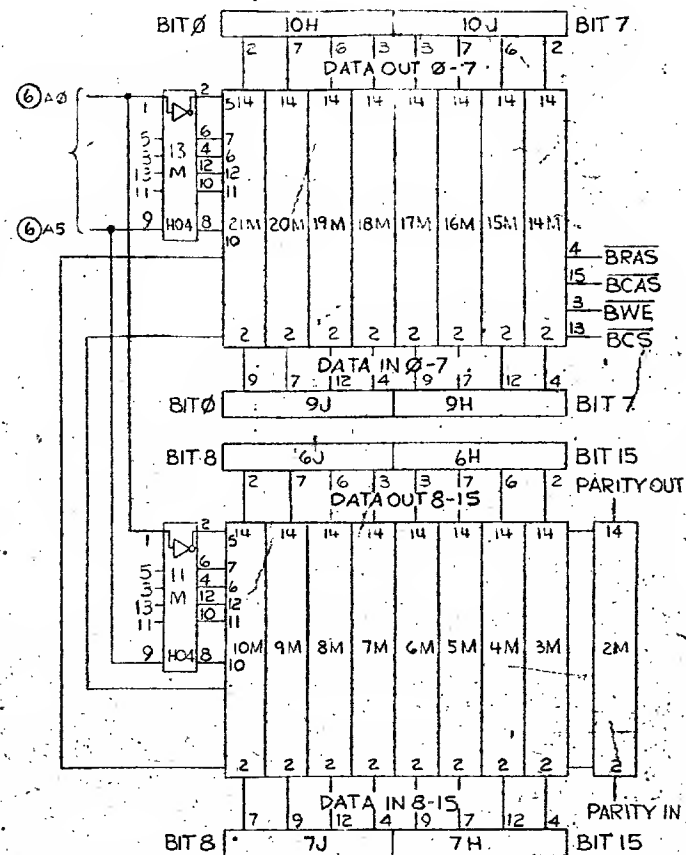
THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.		TOLERANCES DECIMAL XX .XX XXX .XXX FRACTIONAL 3/16 ANGULAR .004		SYN REVISION DESCRIPTION APPRO DATE	
MATERIAL		CHK ENGR PROJ		TITLE 32K MEMORY MODULE SCHEMATIC E-20	
PART NUMBER SEE SHT 1		NEXT ASSEMBLY QTY		SCALE ONE	
COMPUTERVISION CORP. SOUTH AVENUE BURLINGTON, MASS. 01803		SIGNATURE DATE REMOVE ALL BURRS AND SHARP EDGES		UNIT WT.	



MEMORY ARRAY

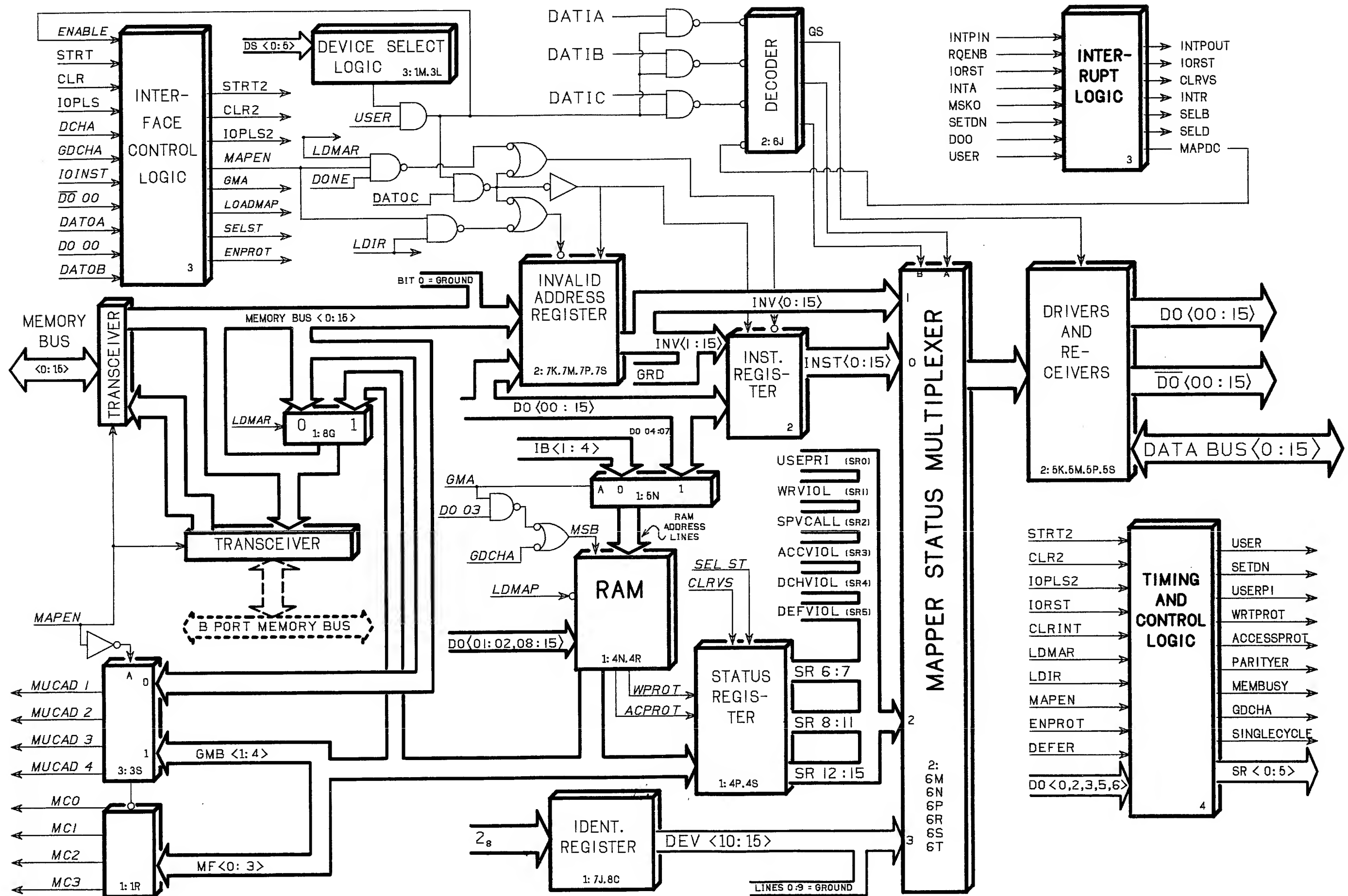
FOR MORE DETAIL OF TYPICAL
4K MEMORY SEE SHEET 5.
FOR MEMORY DATA INPUT/OUTPUT
INTERCONNECTIONS, SEE SHEET 1.

NOTE:
ALL PWR. PINS ON 4027-P3 OR N3 ARE:
+5V PIN 9
-5V PIN 1
GND PIN 16
+12V PIN 8



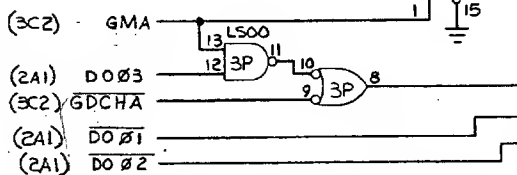
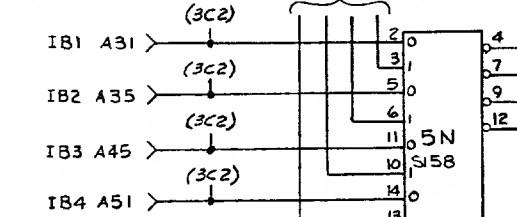
Memory Management and Protection Unit

	<u>Sheet No.</u>
Block Diagram	
Mapper RAM	1
Bus Logic	1
Mapper Status	2
I/O Logic	3
Timing Logic	4
Protection Logic	4

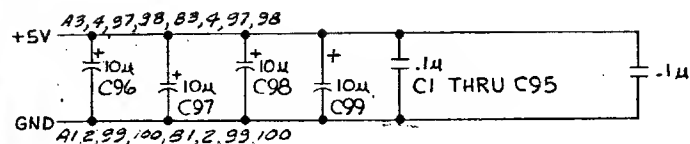


(3B2) LOAD MAP

DO07 - DO04 (2A1), (4A2)



DO07 - DO04 (2A1), (4A2)



NOTES:

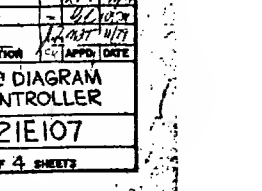
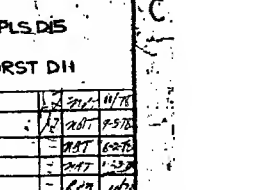
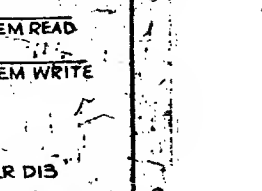
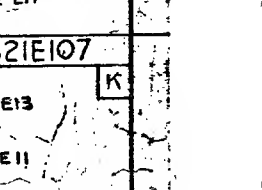
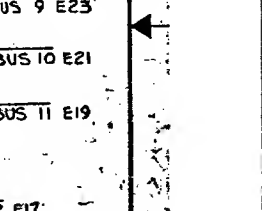
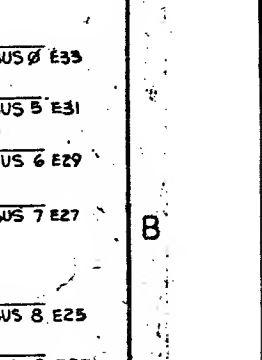
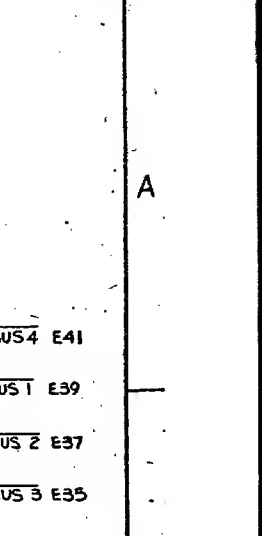
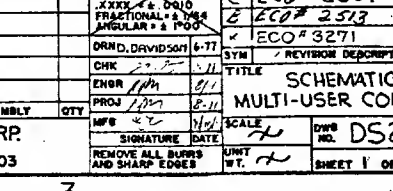
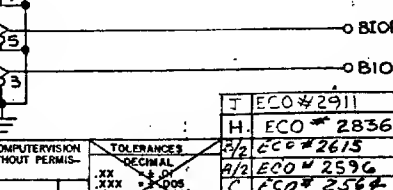
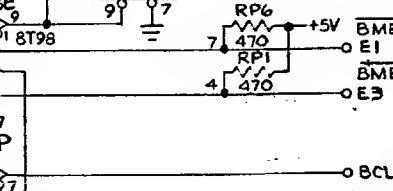
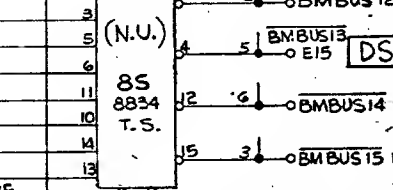
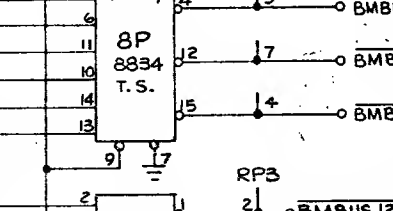
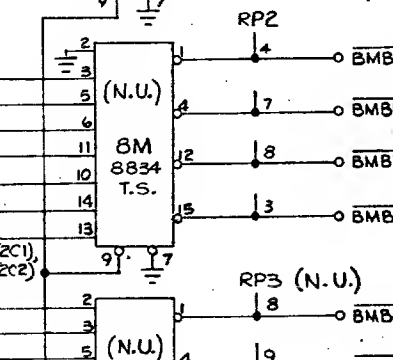
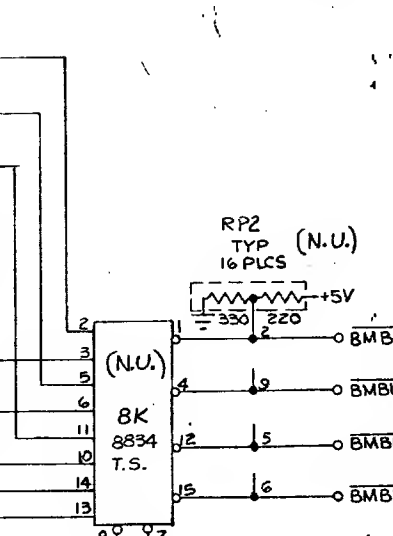
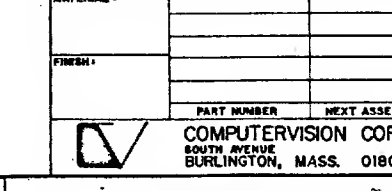
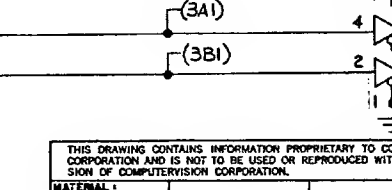
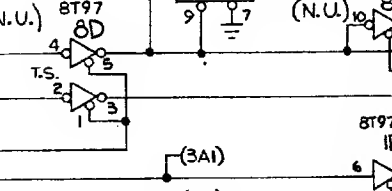
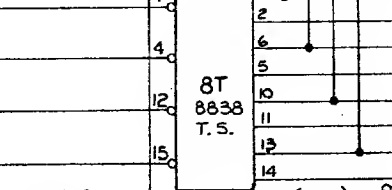
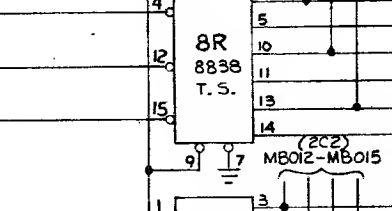
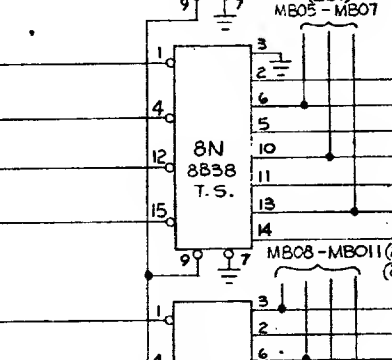
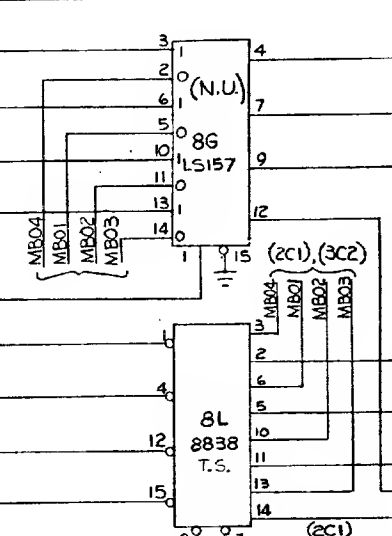
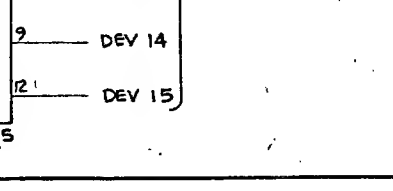
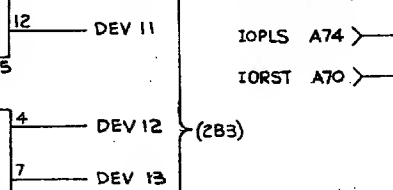
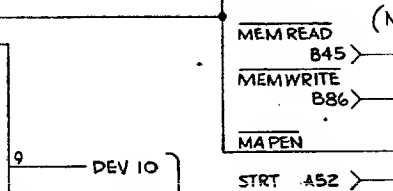
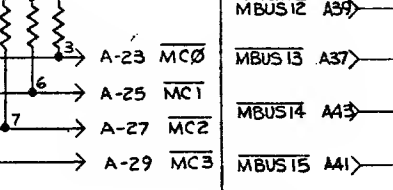
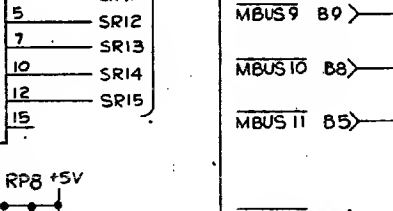
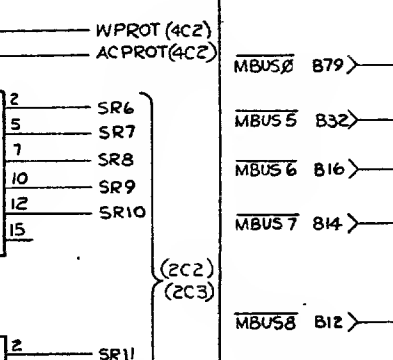
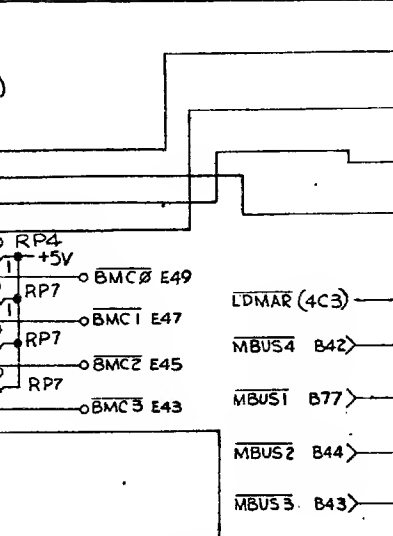
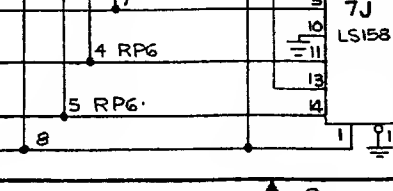
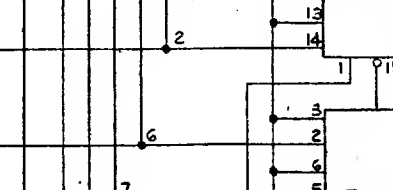
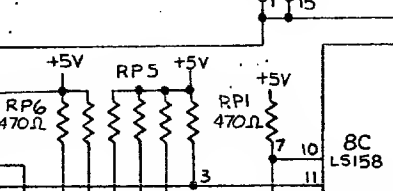
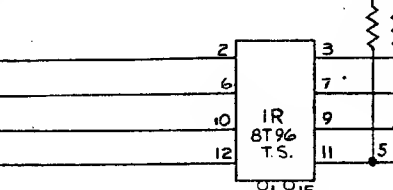
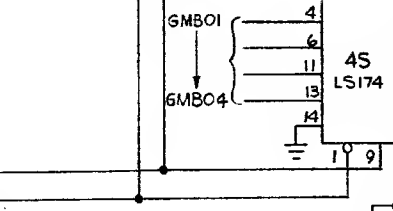
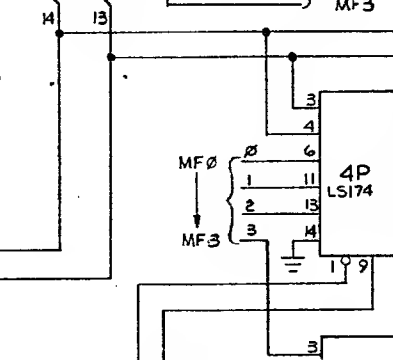
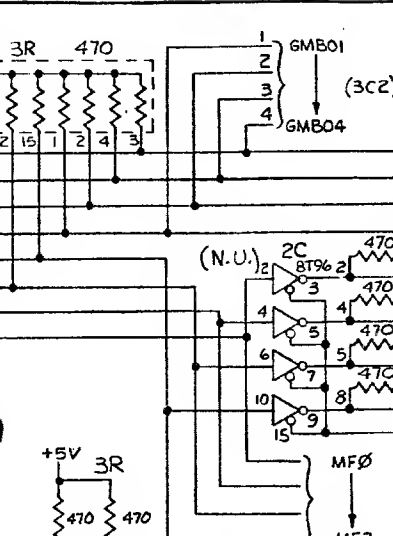
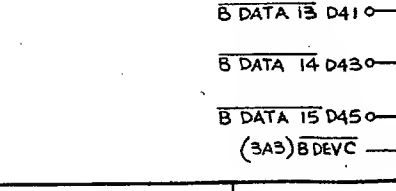
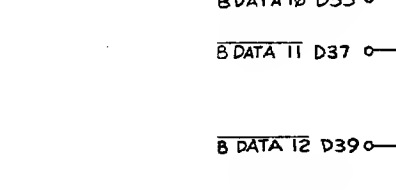
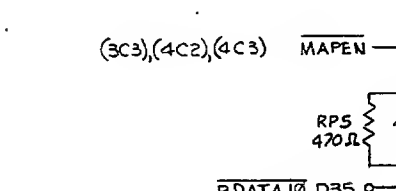
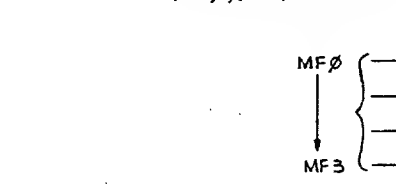
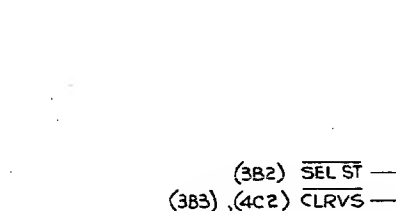
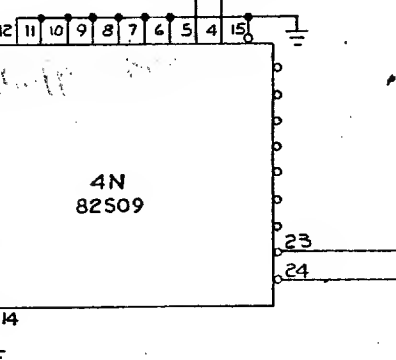
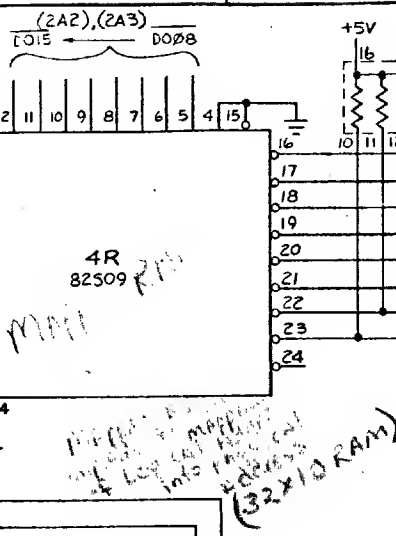
1. FOR SHEET TO SHEET CONNECTIONS ZONES ARE USED:

EX. SHEET COLUMN ROW
(3A2)

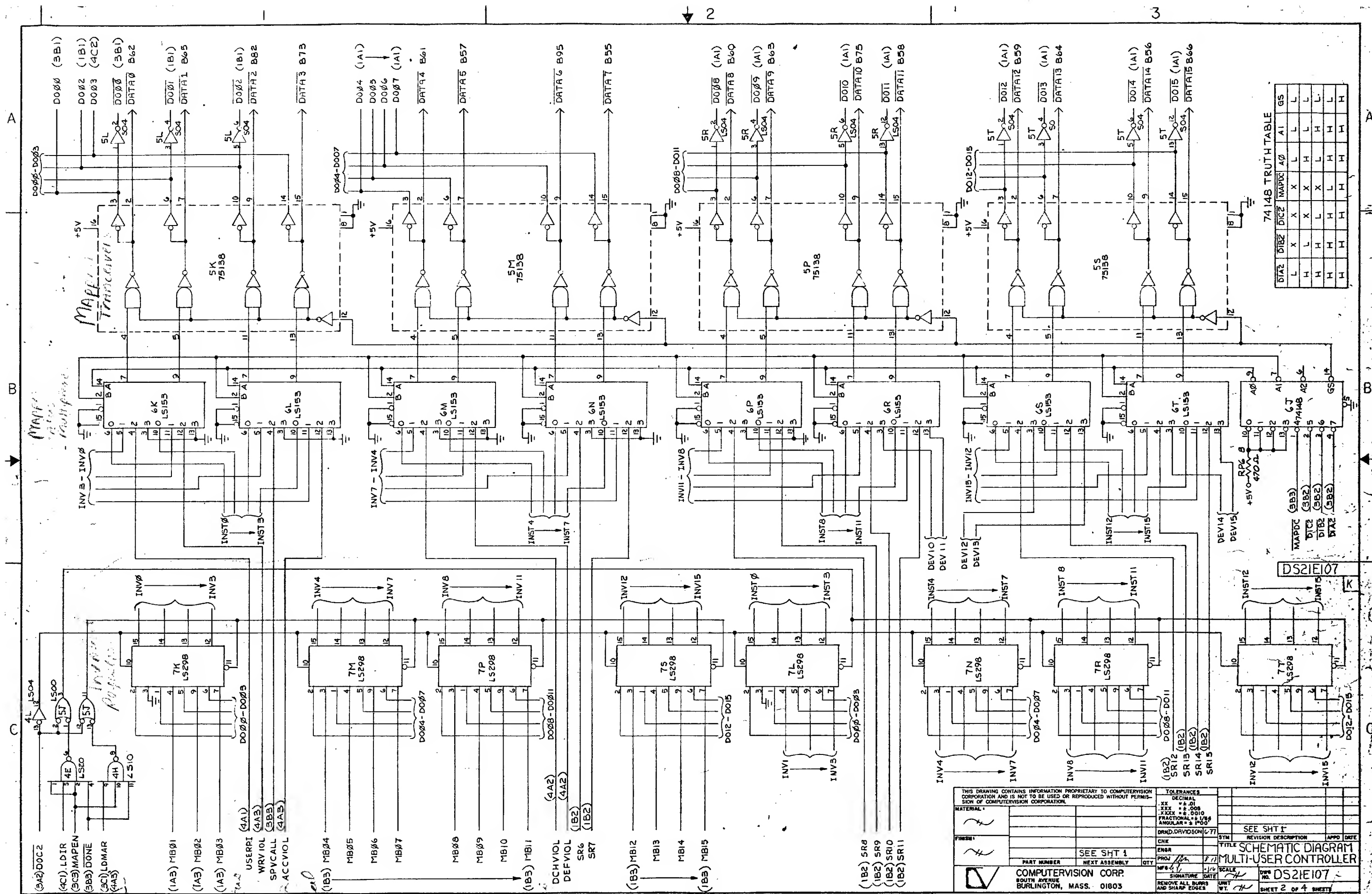
2. UNLESS OTHERWISE SPECIFIED:

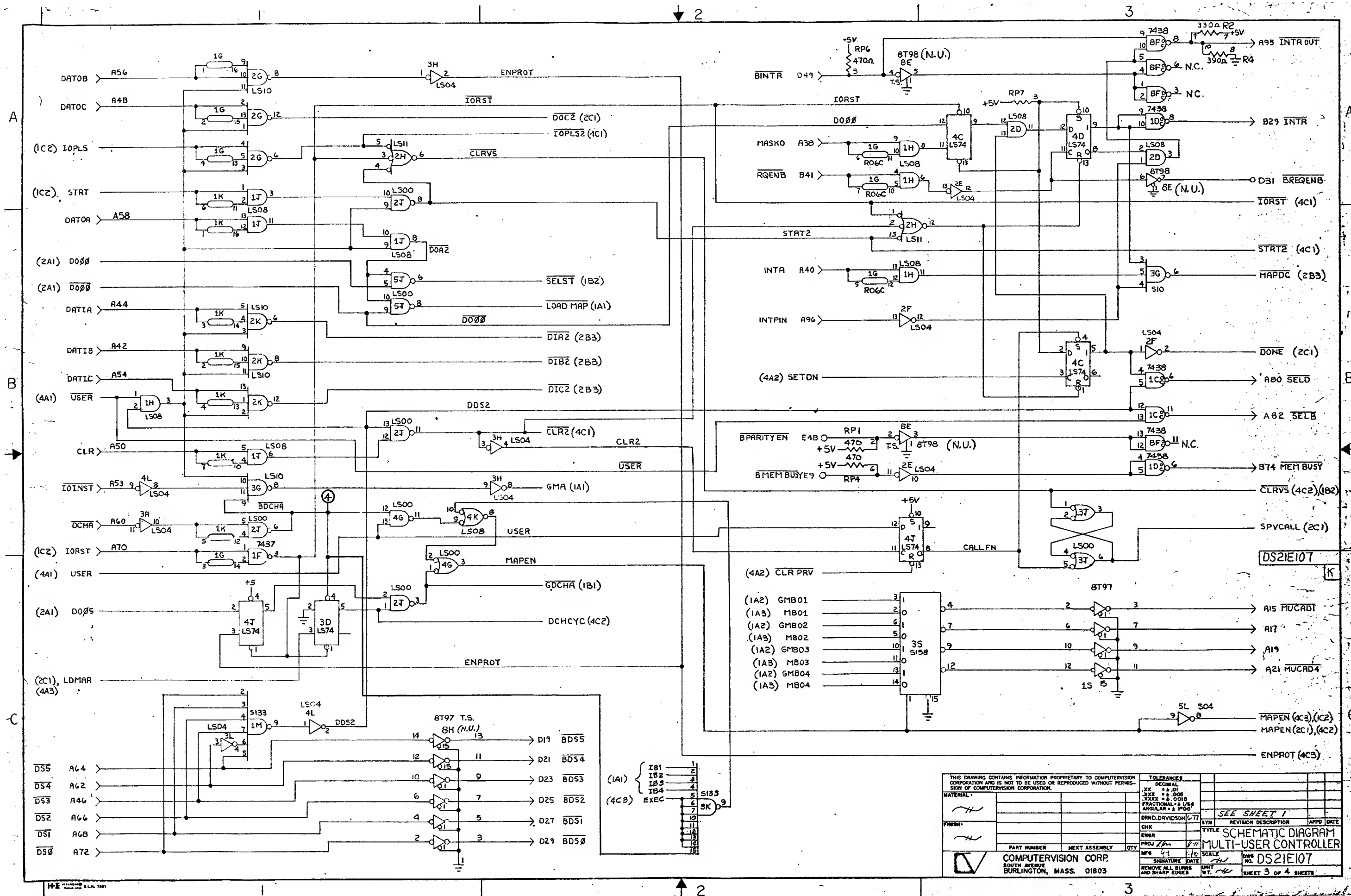
a. ALL RESISTORS ARE 1/4W, 5%
b. ALL CAPACITORS ARE IN MICROFARADS

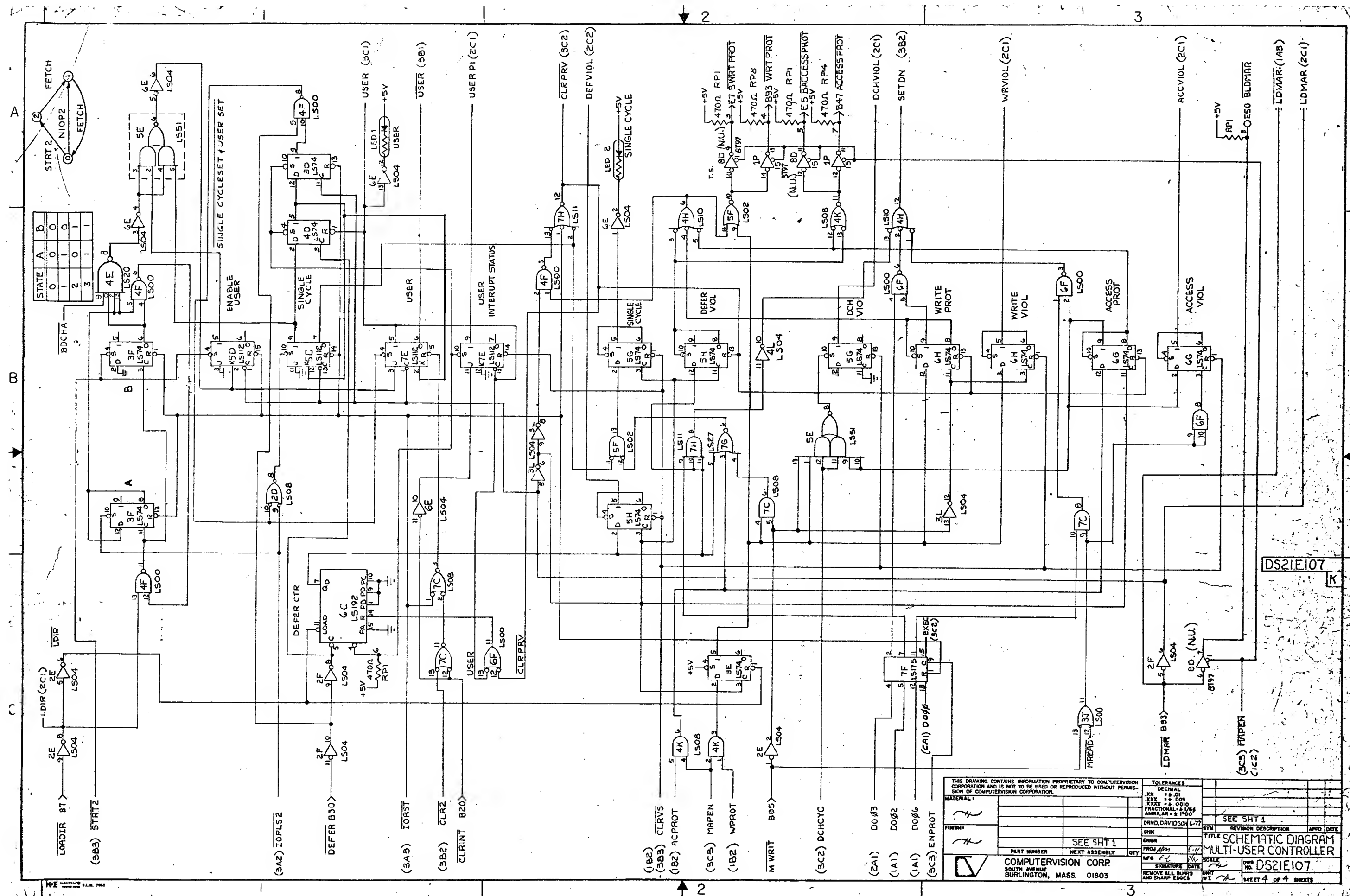
3. FOR PCB ASSEMBLY SEE DWG A21E105



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MATERIAL		DECIMAL	
FINISH		FRACTIONAL	
PART NUMBER		SYMBOL	
NEXT ASSEMBLY		REVISION DESCRIPTION	
QTY		DATE	
COMPUTERVISION CORP.		TITLE	
BURLINGTON, MASS. 01803		SCHEMATIC DIAGRAM	
REMOVE ALL BURRS AND SHARP EDGES		MULTI-USER CONTROLLER	
UNIT WT.		SHEET 1 OF 4 SHEETS	

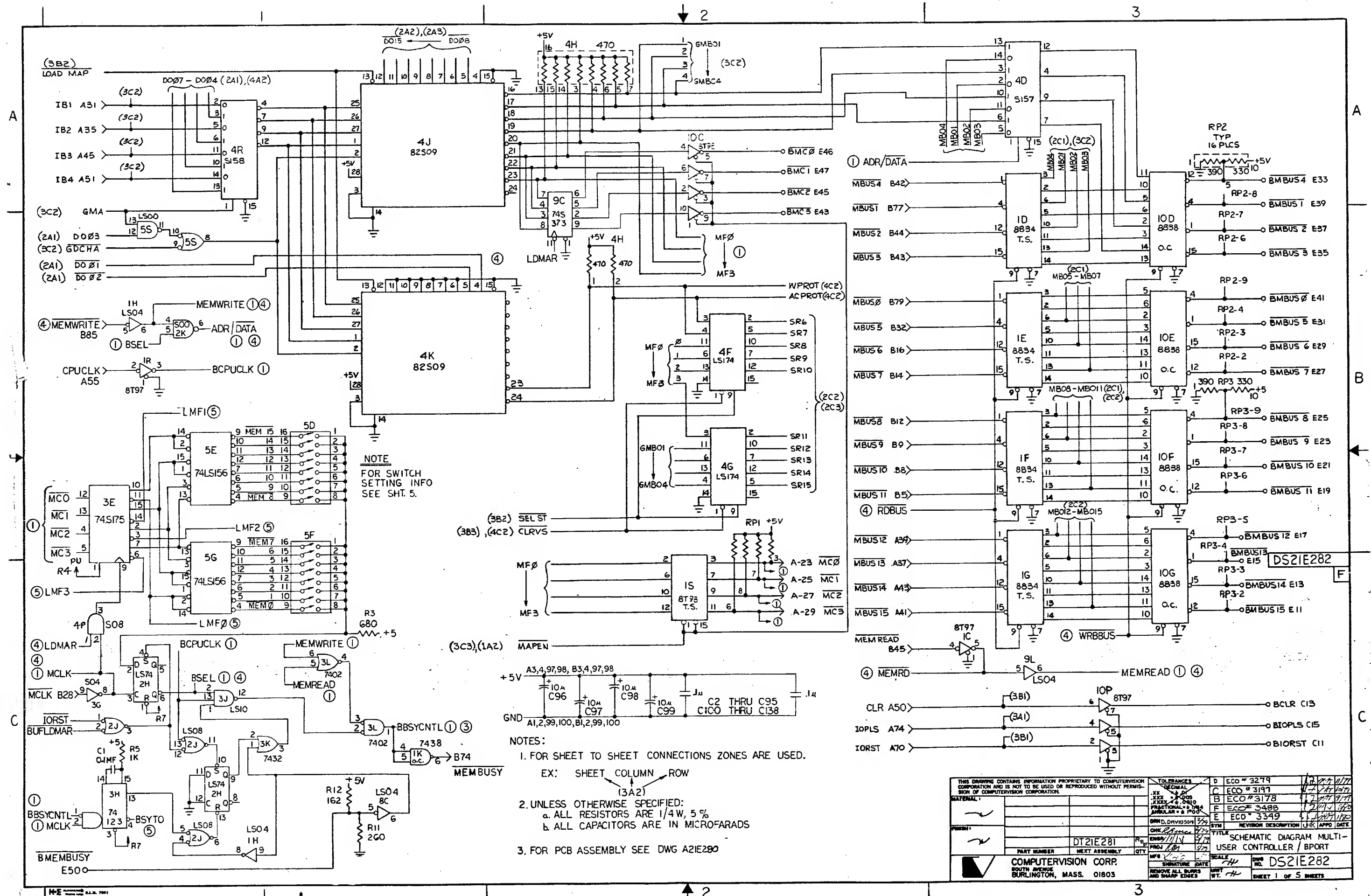


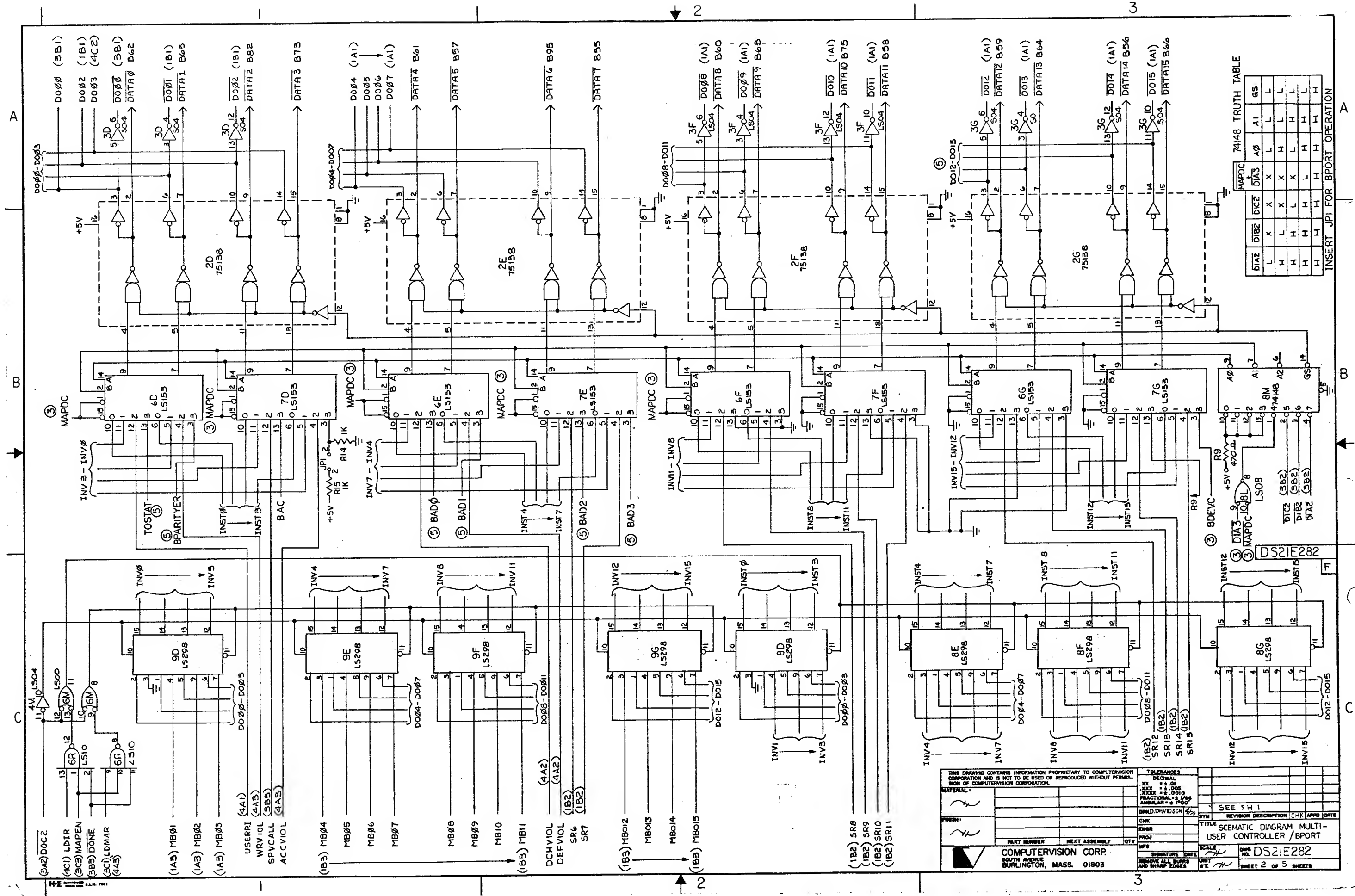


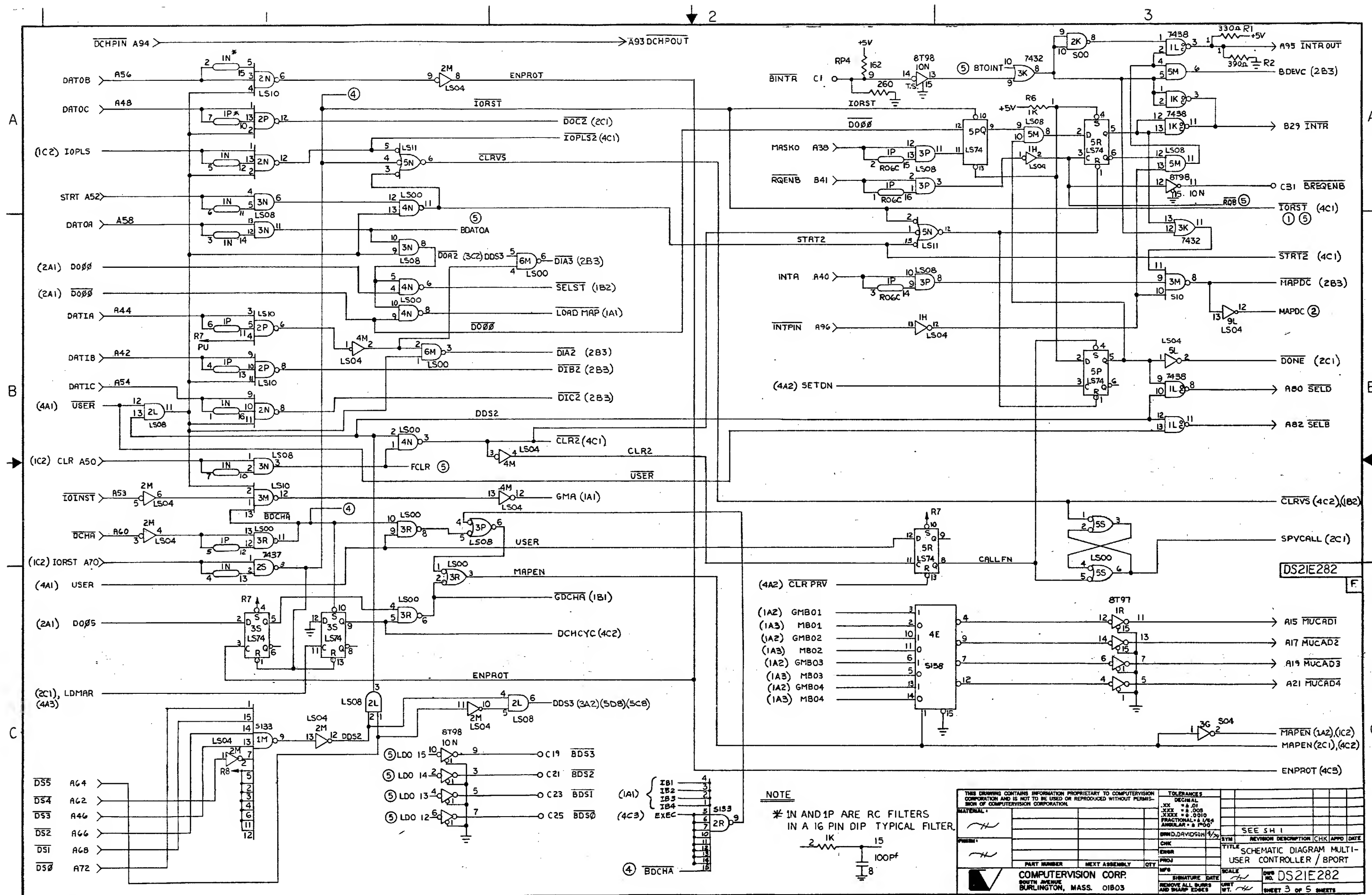


B-Port Memory Management and Protection Unit

	<u>Sheet No.</u>
Mapper RAM	1
Bus Logic	1
Mapper Status Logic	2
I/O Logic	3
Timing Logic	4
Protection Logic	4
Switch Settings	5
Jumper Configuration	5
B-Port Connector Pinouts	5



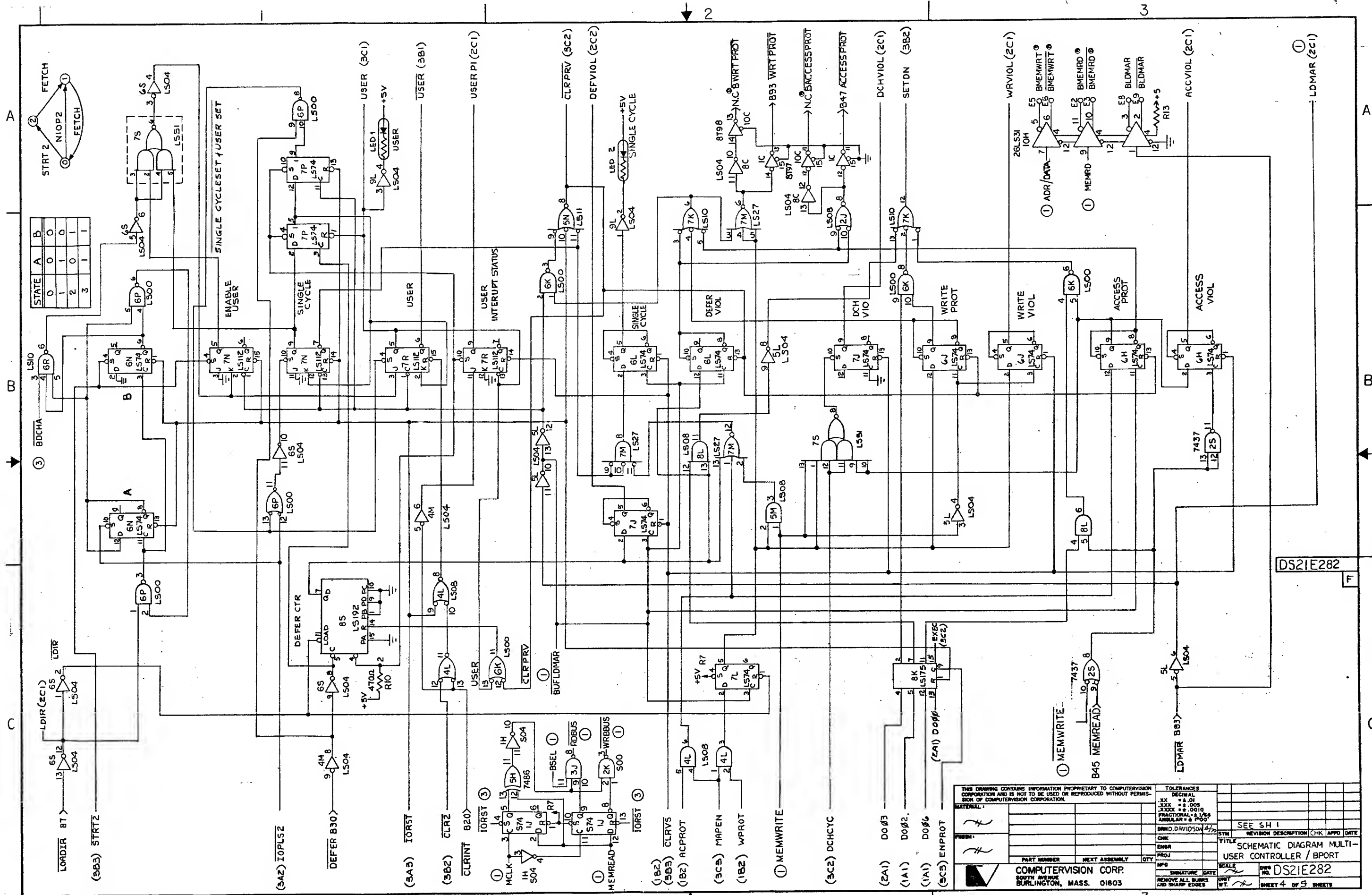




NOTE
* IN AND 1P ARE RC FILTERS
IN A 16 PIN DIP TYPICAL FILTER.

2K 1K 15
100pF

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MATERIAL:		CHK		REVISION DESCRIPTION (CHK APPD DATE)	
PART NUMBER		NEXT ASSEMBLY		QTY	
COMPUTERVISION CORP. SOUTH AVENUE BURLINGTON, MASS. 01803		SIGNATURE DATE		SCALE	
DRAWN: DAVIDSON		CHECKED: [Signature]		DATE: [Date]	
TITLE SCHEMATIC DIAGRAM MULTI- USER CONTROLLER / BPORT		Dwg No.		DS2IE282	
SHEET 3 OF 5 SHEETS					



STATE

A	B
0	0
1	0
2	0
3	1

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DATE: 7/77

REVISION: 1

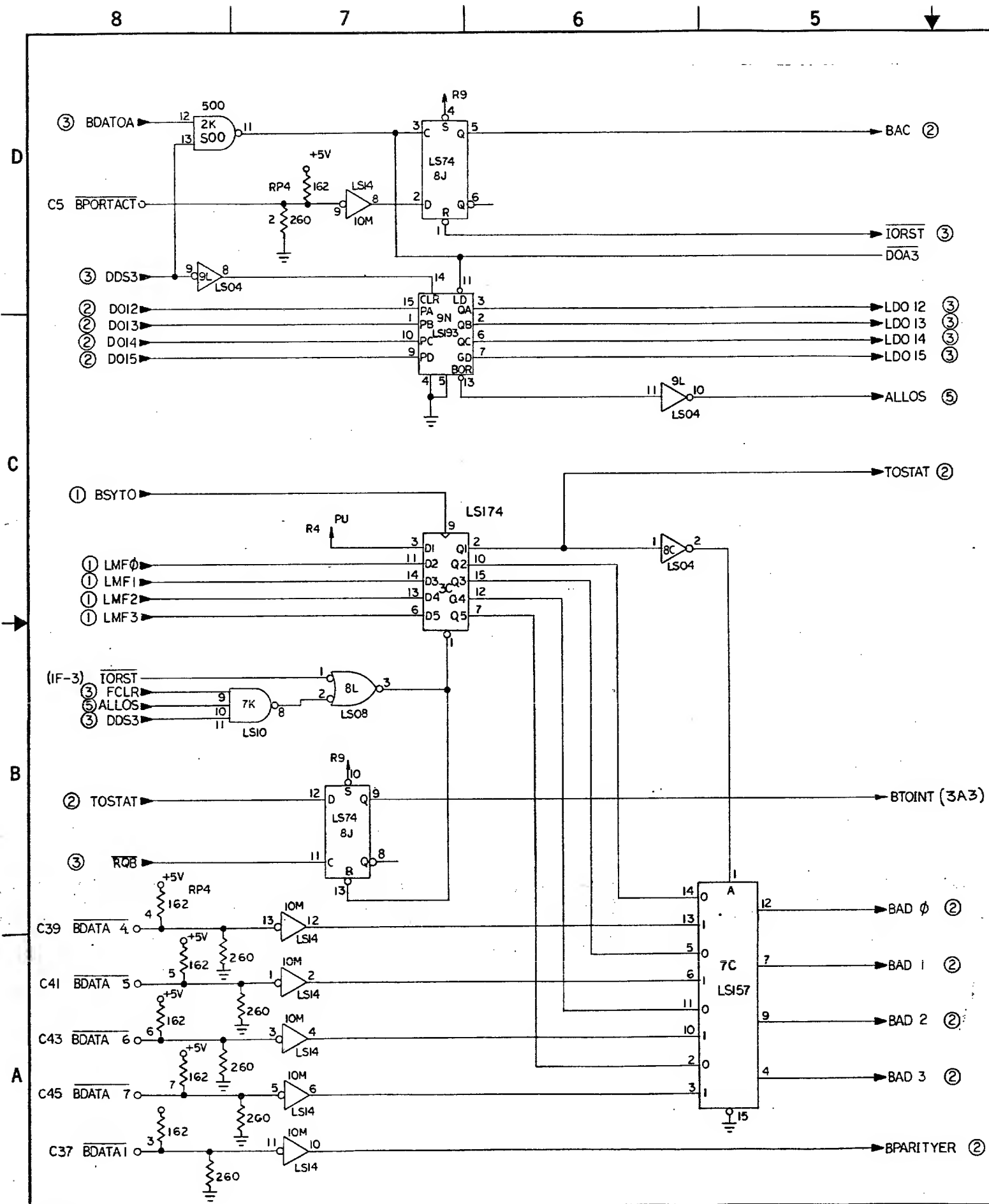
REVISION DESCRIPTION: SEE SH 1

TITLE: SCHEMATIC DIAGRAM MULTI-USER CONTROLLER / BPORT

SCALE: 1/8"

SHEET 4 OF 5 SHEETS

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803



SWITCH PACKS 5D & 5F

THE PROPER SWITCHES IN SWITCH PACKS 5D & 5F MUST BE CLOSED WHEN THE MUC IS DRIVING BPORT MEMORIES. ONE SWITCH MUST BE CLOSED FOR EVERY 32K BPORT FIELD SEGMENT ADDRESS THAT IS BEING USED IN A CONFIGURED SYSTEM.

BPORT FIELD ADDR*	CLOSED SWITCH POSITION	
	5D	5F
0		8
1		7
2		6
3		5
4		4
5		3
6		2
7		1
8	8	
9	7	
10	6	
11	5	
12	4	
13	3	
14	2	
15	1	

* THE BPORT FIELD ADDR REPRESENTS ONE 32K SEGMENT OF MEMORY.

REF SHT.2, JP1 MUST BE INSERTED WHEN THE MUC IS DRIVING BPORT MEMORIES.

B PORT CONNECTOR PINOUTS

CONN C

1	BINTR	2
3		4
5	BPORTACT	6
7		8
9		10
11	BIORST	12
13	BCLR	14
15	BIOPLS	16
17		18
19	BDS3	20
21	BDS2	22
23	BDS1	24
25	BDS0	26
27		28
29		30
31	BROENB	32
33		34
35		36
37	BDATA1	38
39	BDATA4	40
41	BDATA5	42
43	BDATA6	44
45	BDATA7	46
47		48
49		50

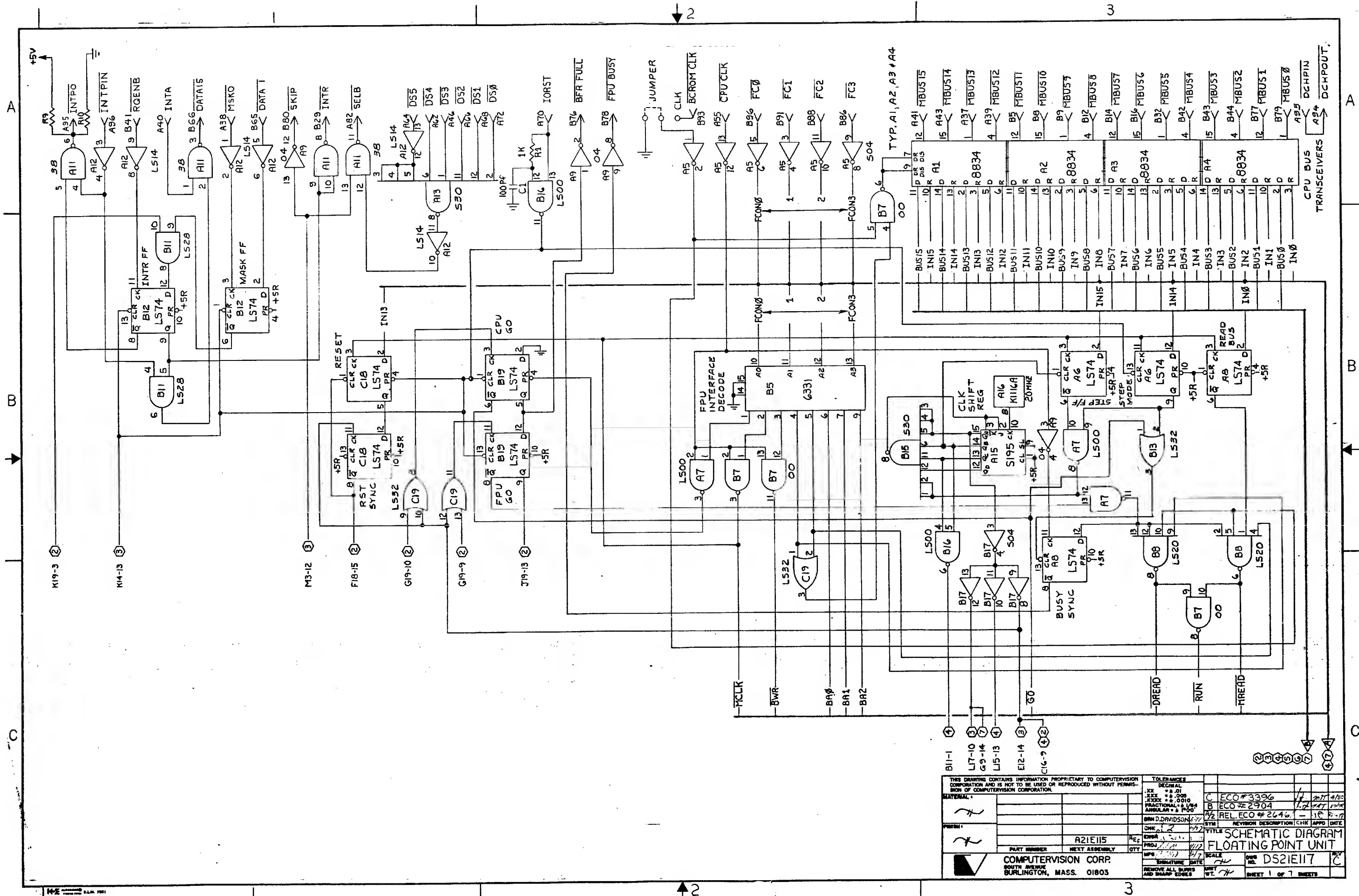
CONN E

1	BMEMRD	2
3	BMEMWRT	4
5	BMEMWRT	6
7	BMDMAR	8
9	BMDMAR	10
11	BMEMBUS15	12
13		14
15		16
17		18
19		20
21		22
23		24
25		26
27		28
29		30
31		32
33		34
35		36
37		38
39		40
41	BMEMBUS0	42
43	BMC3	44
45	BMC2	46
47	BMC1	48
49	BMEMBSY	50

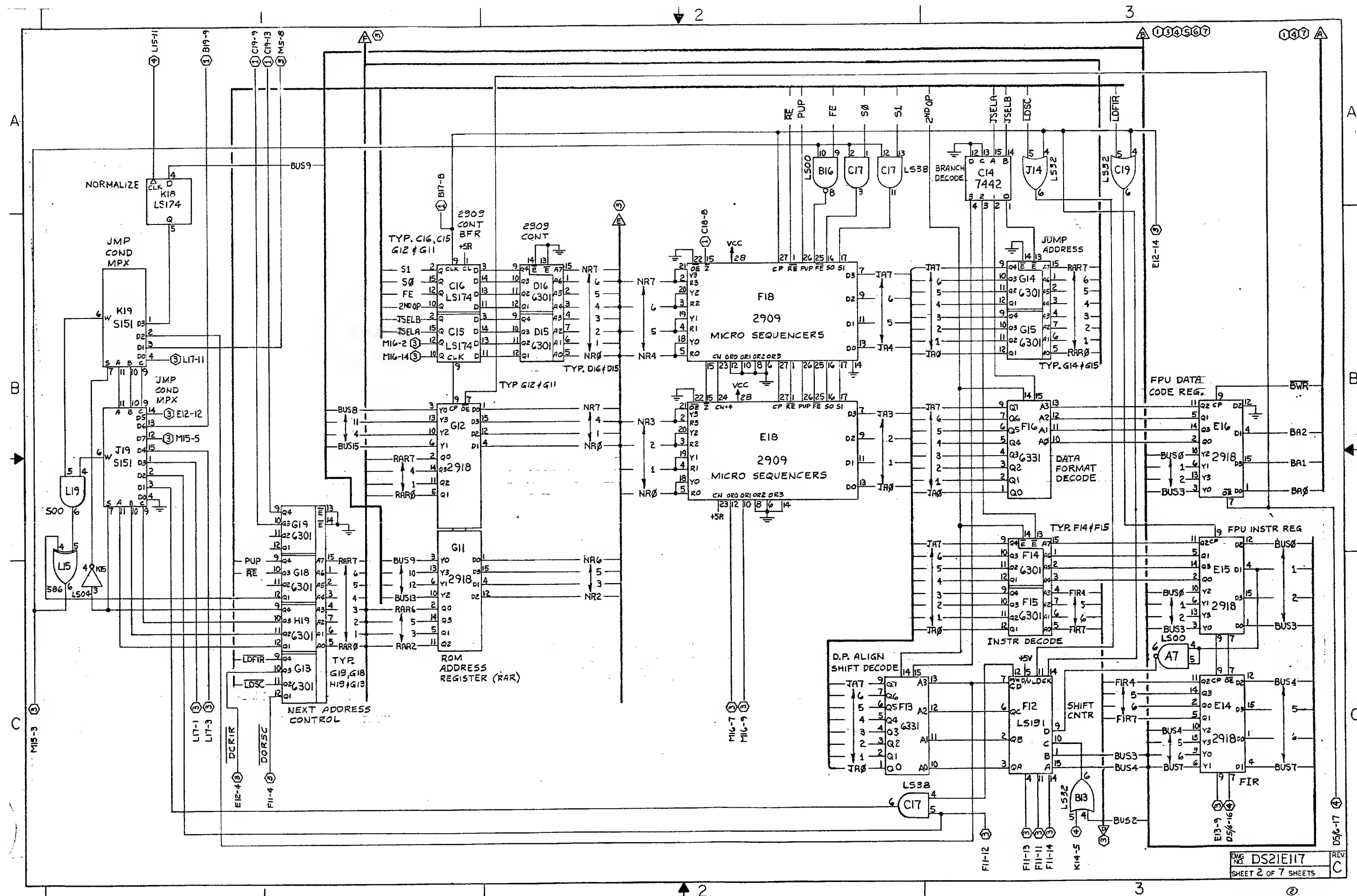
ALL UNUSED PINS GROUNDED

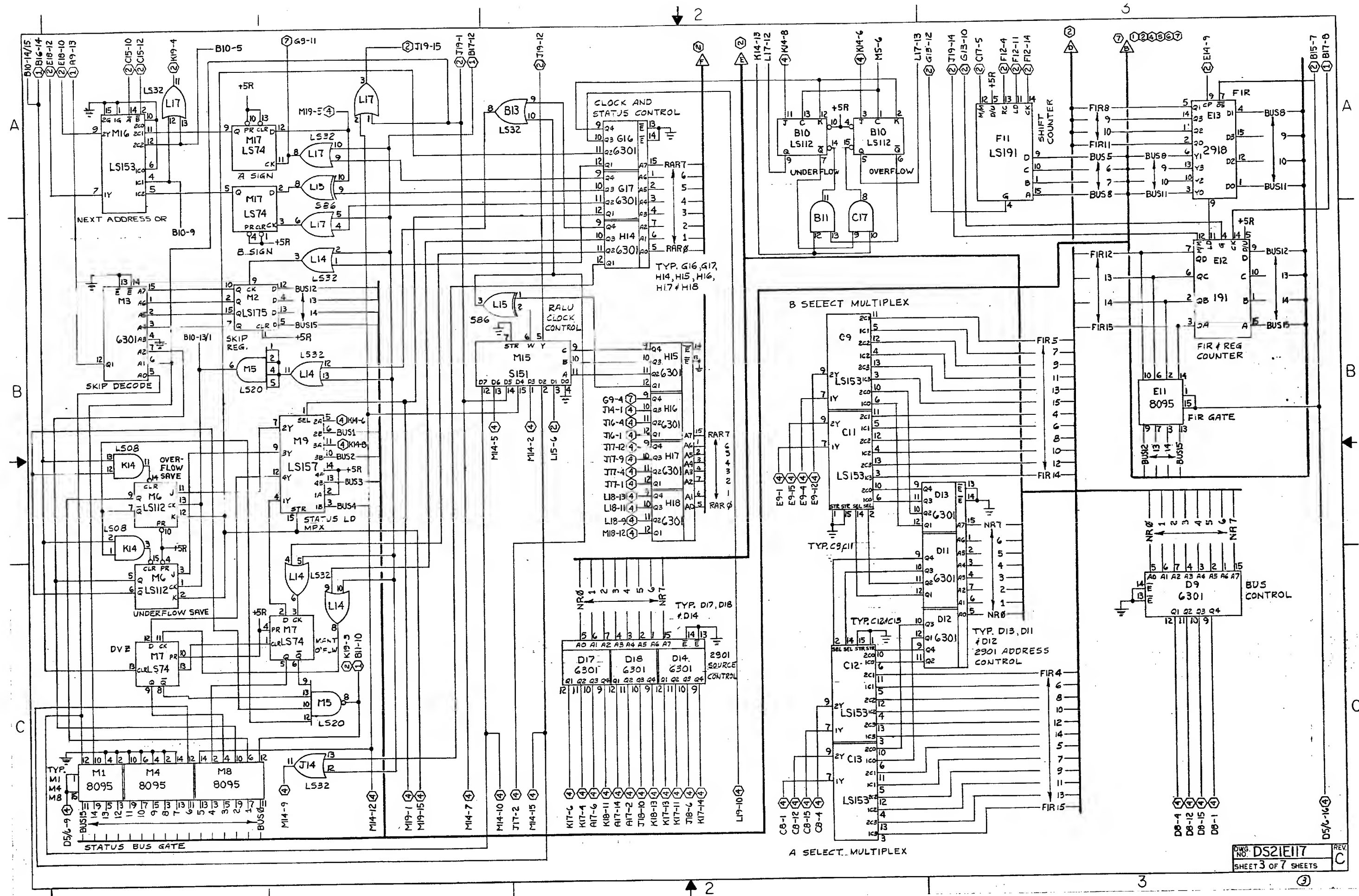
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MATERIAL:		CHK	DATE	SYN	REVISION DESCRIPTION
PREP:		CHK	DATE	SYN	REVISION DESCRIPTION
PART NUMBER	NEXT ASSEMBLY	QTY	TITLE SCHEMATIC DIAGRAM MULTI- USER CONTROLLER / BPORT		
COMPUTERVISION CORP. 301 Burlington Road Bedford, Massachusetts 01730			DWG NO. DS2IE282 SHEET 5 OF 5 SHEETS		

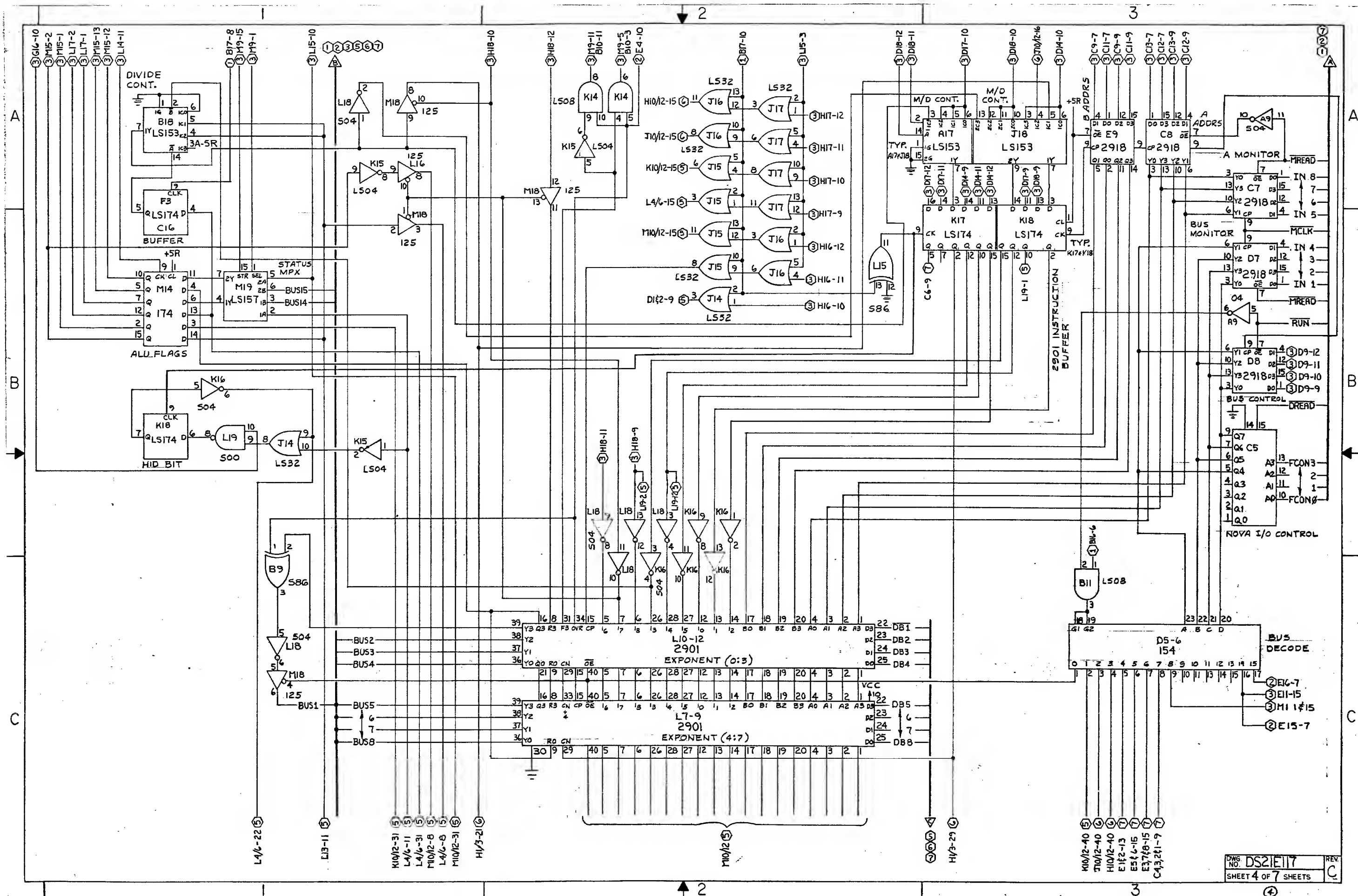
Floating Point Unit

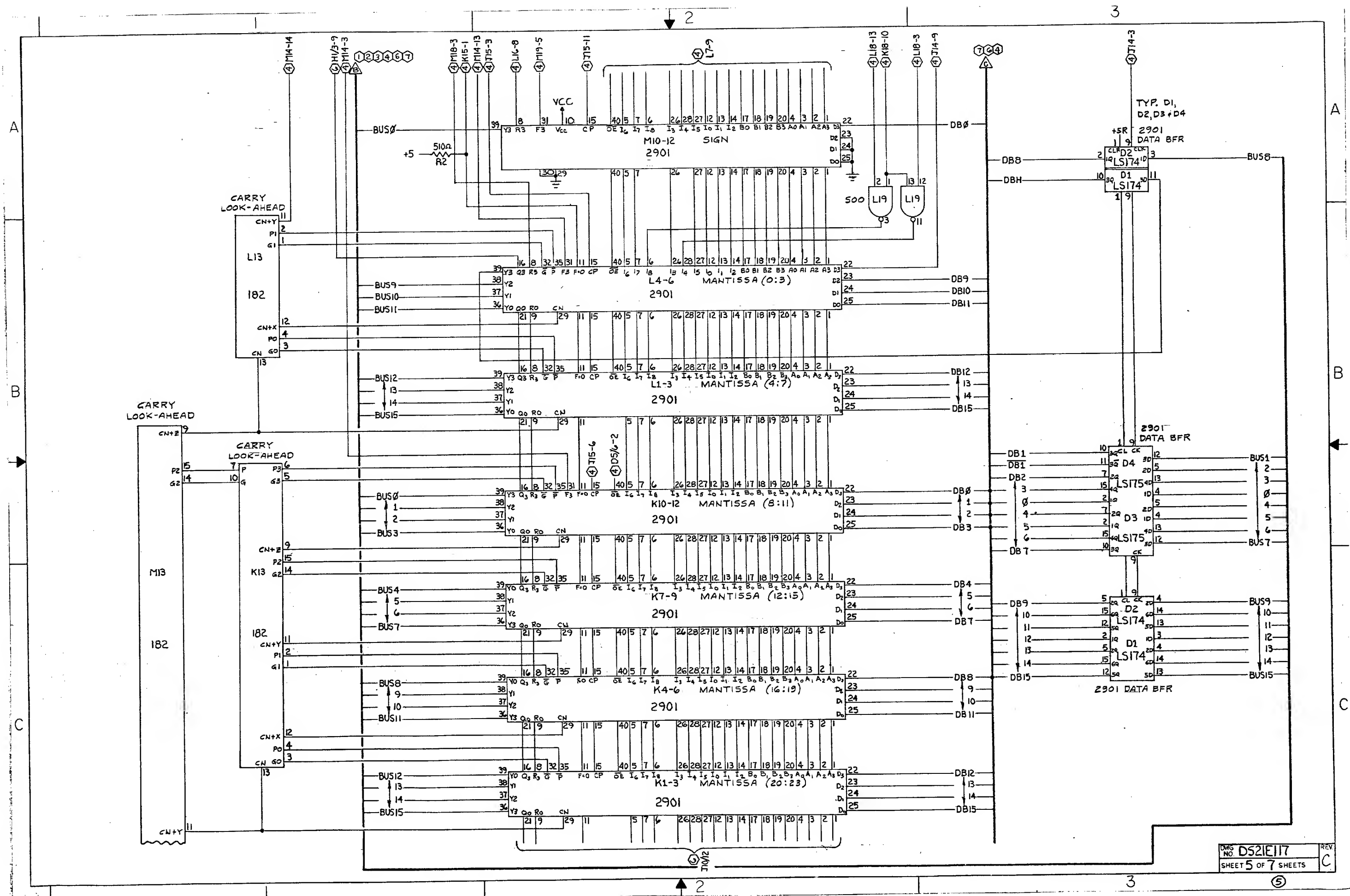


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MATERIAL		BY D. DAVIDSON		SYN	
PART NUMBER		NEXT ASSEMBLY		QTY	
COMPUTERVISION CORP. SOUTH AVENUE BURLINGTON, MASS. 01803		SCALE		UNIT	
REWORK ALL BURNS AND SHARP EDGES		SHEET 1 OF 7 SHEETS		REV	









A

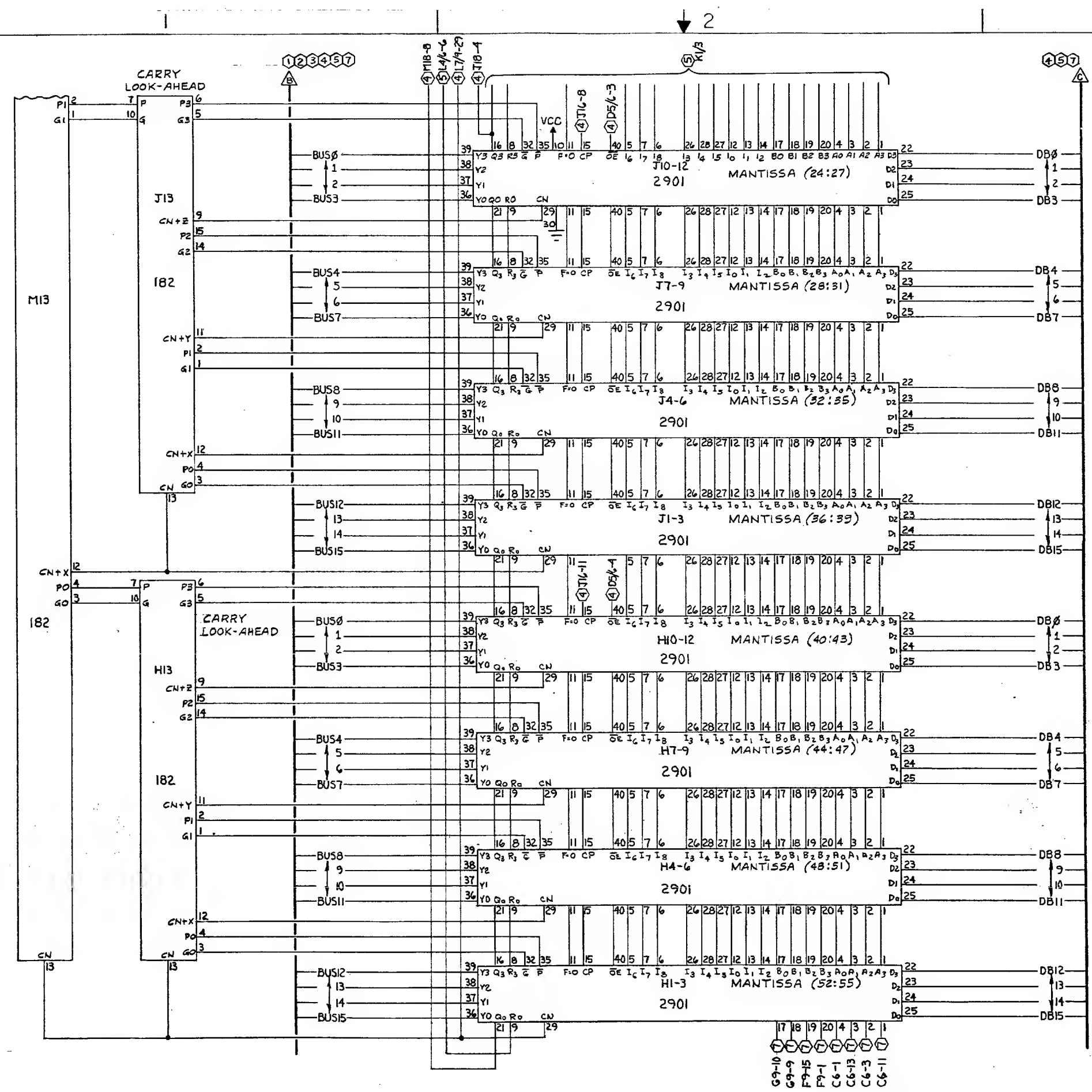
B

C

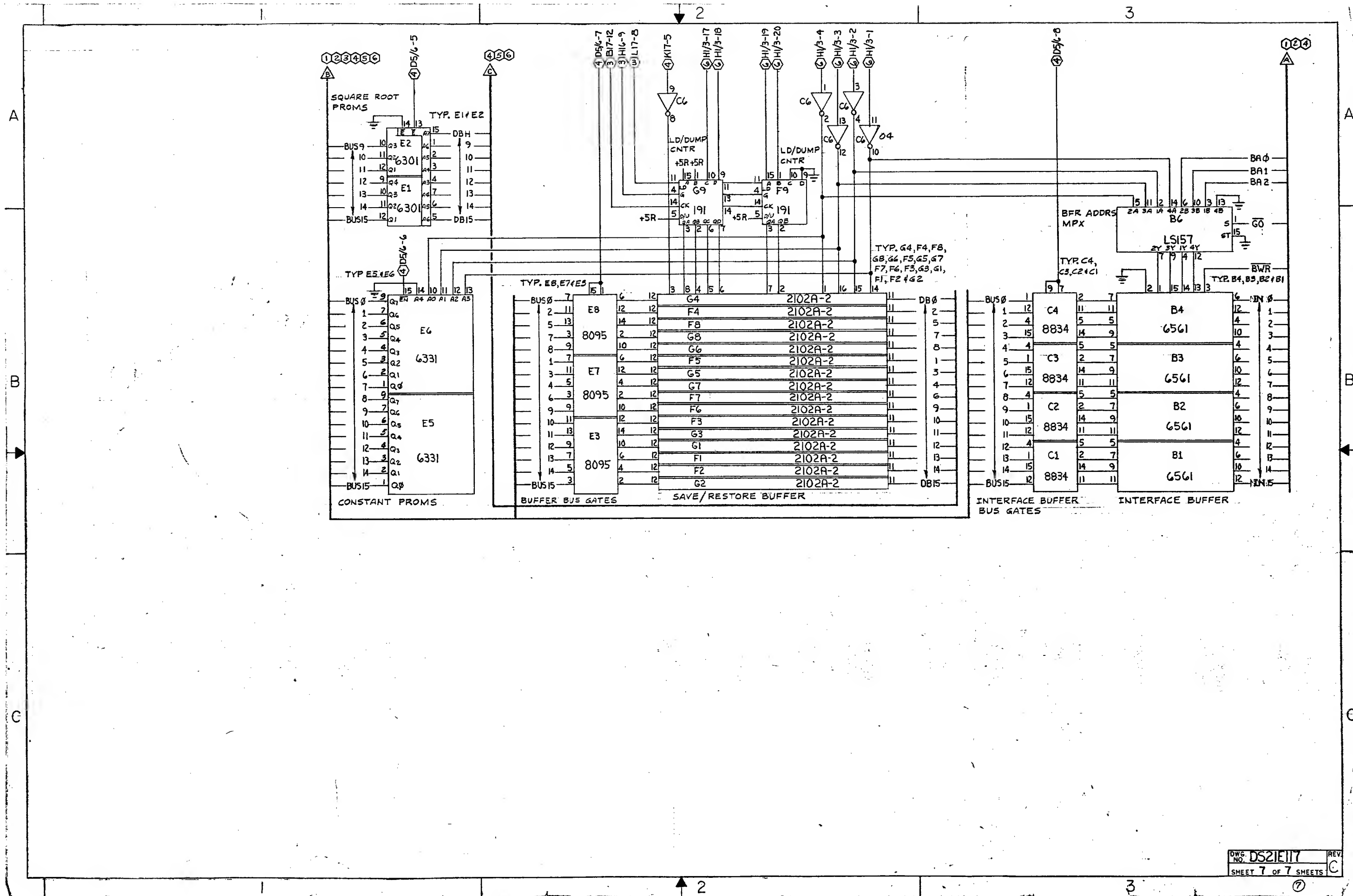
A

B

C



17 18 19 20 4 3 2 1
GND GND GND GND GND GND
GND GND GND GND GND GND



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